ZiLOG

Totally Logical

Z90371/376

DUAL-SCAN DIGITAL TV CONTROLLER FOR PROGRESSIVE DOUBLE-SCAN APPLICATIONS

DESCRIPTION

Supporting progressive-scan, double-scan, and interlaced modes of operation, ZiLOG's Z9037X family of microcontrollers provide a highly-integrated solution for any TV. As a stand-alone controller, the Z9037X provides the most cost-effective TV control and On-Screen Display (OSD) available. Designed with a high-speed 16-bit DSP controller, this device allows the ultimate OSD flexibility for digital VBI data capture. The power of the Z9037X architecture is supported by a variety of OSD applications including V-Chip, XDS, and Line 21 closed captioning.

FEATURES

On Screen Display (OSD) Features

- Supports three modes: OSD progressive-scan non-interlaced mode, OSD double-scan interlaced mode, and OSD interlaced-scan standard mode
- Programmable foreground and background colors by character
- Relocates the CGROM with the number of fonts and characters only limited by the available ROM memory
- Supports 16x16, 16x18, and 16x20 pixel size
- OSD support programmable, with 4 colors per pixel hardware cursor (sprite) and pixel-by-pixel position control
- Supports semi-trandparent, blinking, multi-color icon, italic, bold, and underline on a character-by-character basis
- Supports Closed Captioning and display in accordance with the FCC Report and Order on GEN Docket No. 91–1 (dated April 12, 1991). This feature allows Extended Data System (XDS) capability to be easily implemented
- Advanced TV controller IC with sophisticated OSD capability and integral VBI data decoding

TV Control Features

- Infrared remote (IR) capture register that facilitates reliable capture of remote data—even in high-noise environments
- 6-Channel, 4-bit Analog-to-Digital Converter (ADC)
- 6 PWM (Pulse Width Modulator) outputs that allow low-cost digital to analog conversion
- Master/Slave Inter-Integrated Circuit[1] (I^2C) bus interface that provides a serial system interconnect to common peripheral functions
- Bit-programmable I/O ports that provide flexibility for miscellaneous digital input/output functions

Microcontroller Features

- 16-Bit single-cycle instruction execution DSP core that provides fast instruction throughput
- 24.0-MHz nominal Phase Lock Loop (PLL) controlled oscillators that provide stable system and video clocks. Only one external capacitor is required for the loop filter function. A 32.768-KHz oscillator is used for reference
- Available in 52-pin SDIP with 64K Words ROM size

Development Tools & Support

- Available in One Time Programmable (OTP) and MASK ROM versions to fulfill prototype and production requirements
- Supported by ICEbox[2] in-circuit tools for programming and debug.
- ZiLOG Application Programmer Interface (API) is a set of device drivers, state machines, and collection of library object code[3].

[1] Philips standard serial interface.
[2] ZiLOG, Inc. family of in-circuit emulators.
[3] The API deals directly with the proper sequence and timing when interfacing with the hardware, shielding the user application program from tedious and error prone details.

GENERAL DESCRIPTION

This controller supports progressive-scan, double-scan, and interlaced OSD modes. ZiLOG's Z9037X family provides a highly-integrated solution for TV design. Designed with a high-speed 16-bit DSP controller, this device provides the ultimate in OSD flexibility. This architecture is supported by a variety of OSD capabilities including hardware cursor, semi-transparency, and programmable color palettes.The Z9037X supports V-Chip, Extended Data System (XDS), and Line 21 closed captioning in software. No additional hardware is required.

Table 1. Z9037X Device Selection

Device	Application	ROM (words)	RAM (words)	Pkg.	I2C	Cursor	2X Pixel Rate	IR Capture	ADC	Bit I/O (max)	PWM
Z90371	TV receiver controller	64K OTP	1024	52-pin SDIP	1M/1S	Yes	Yes	Yes	6ch	25	6
Z90376	TV receiver controller	64K ROM	1024	52-pin SDIP	1M/1S	Yes	Yes	Yes	6ch	25	6

Parameters

Progressive scan (noninterlaced)	
HSYNC(NTSC)	= 31,468 Hz (31.78 µs)
HSYNC(PAL)	= 31,250 Hz (32 µs)
VSYNC (NTSC)	= 60 Hz (16.67 ms)
VSYNC (PAL)	= 50 Hz (20 ms)
Double scan (interlaced)	
HSYNC(NTSC)	= 31,468 Hz (31.78 µs)
HSYNC(PAL)	= 31,250 Hz (32 µs)
VSYNC (NTSC)	= 120 Hz (8.33 ms)
VSYNC (PAL)	= 100 Hz (10 ms)
Interlaced scan (standard)	
HSYNC(NTSC)	= 15,734 Hz (63.56 µs)
HSYNC(PAL)	= 15,625 Hz (32 µs)
VSYNC (NTSC)	= 60 Hz (16.67 ms)
VSYNC (PAL)	= 50 Hz (10 ms)

This controller supports progressive-scan, double-scan, and interlaced OSD modes. ZiLOG's Z9037X family provides a highly-integrated solution for TV design. Designed with a high-speed 16-bit DSP controller, this device provides the ultimate in OSD flexibility. This architecture is supported by a variety of OSD capabilities including hardware cursor, semi-transparency, and programmable color palettes.The Z9037X supports V-Chip, Extended Data System (XDS), and Line 21 closed captioning in software. No additional hardware is required.

A block diagram of the Z9037X is illustrated in Figure 1.

Note: All Signals with an overline are active Low. For example, B/$\overline{W}$, in which WORD is active Low), and $\overline{B}$/W, in which BYTE is active Low.

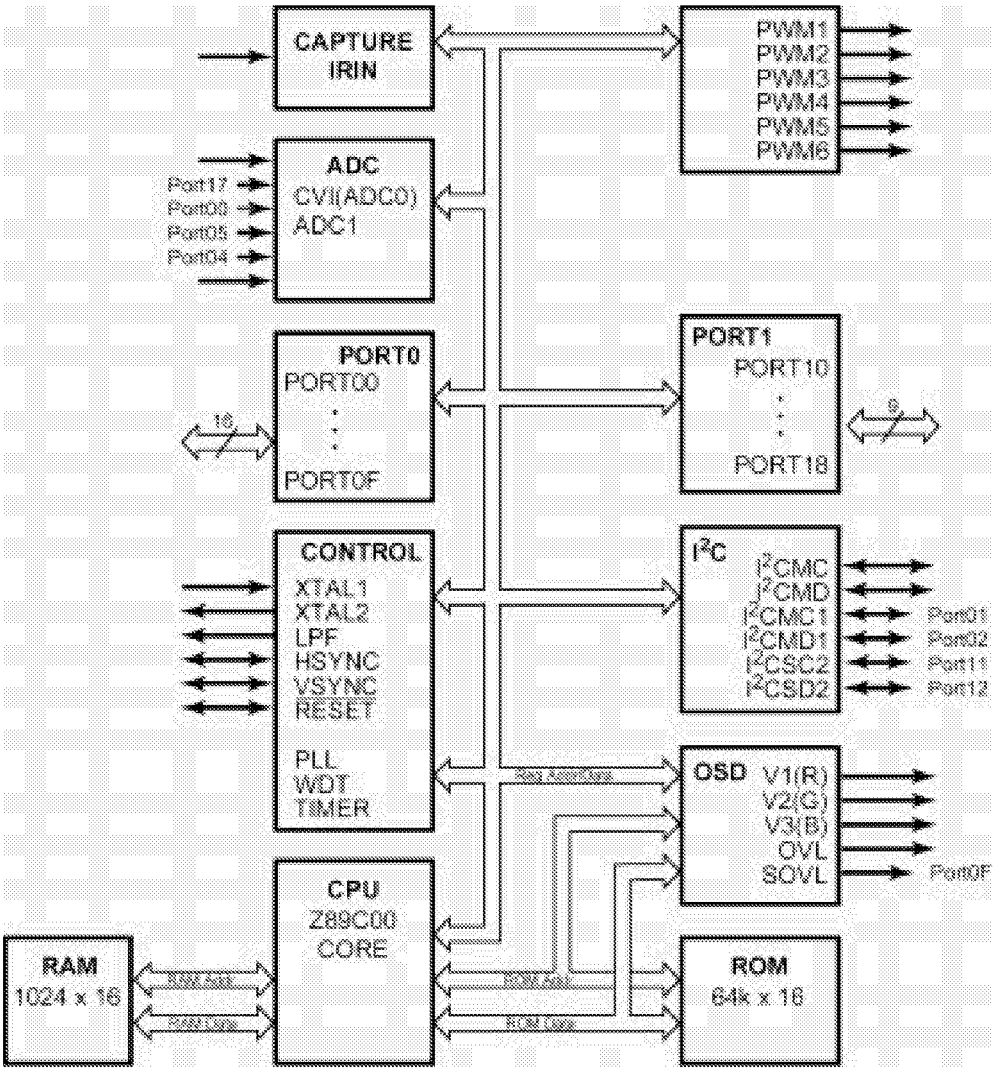


Figure 1. Functional Block Diagram

GENERAL DESCRIPTION (Continued)

Table 2. Z90371/376 52-SDIP Pinout

Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #	Pin Name	Pin #
P16/SCLK	1	LPF	14	OVL	27	GND	40
IRIN	2	AGNDF	15	HSYNC	28	PWM1	41
P0C	3	ADC5	16	VSYNC	29	PWM2	42
P0B	4	P04/ADC4	17	P12/I^2CMD2	30	PWM3	43
P0A	5	P05/ADC3	18	P11/I^2CMC2	31	PWM4	44
P09	6	P00/ADC2	19	P0E	32	PWM5	45
P0D	7	P17/ADC1	20	I^2CMD1	33	PWM6	46
P07/CSYNC	8	AGND	21	I^2CMC1	34	P10/R<0>	47
P06/CNTR	9	AVCC	22	RESET	35	P08/R<1>	48
P03/1xHSYNC	10	P0F/SOVL	23	XTAL1	36	P18/G<0>	49
P01/I^2CSC	11	V3 (B)	24	XTAL2	37	P13/G<1>	50
P02/I^2CSD	12	V2 (G)	25	GND	38	P14/B<0>	51
CVI/ADC0	13	V1 (R)	26	VCC	39	P15/B<1>	52

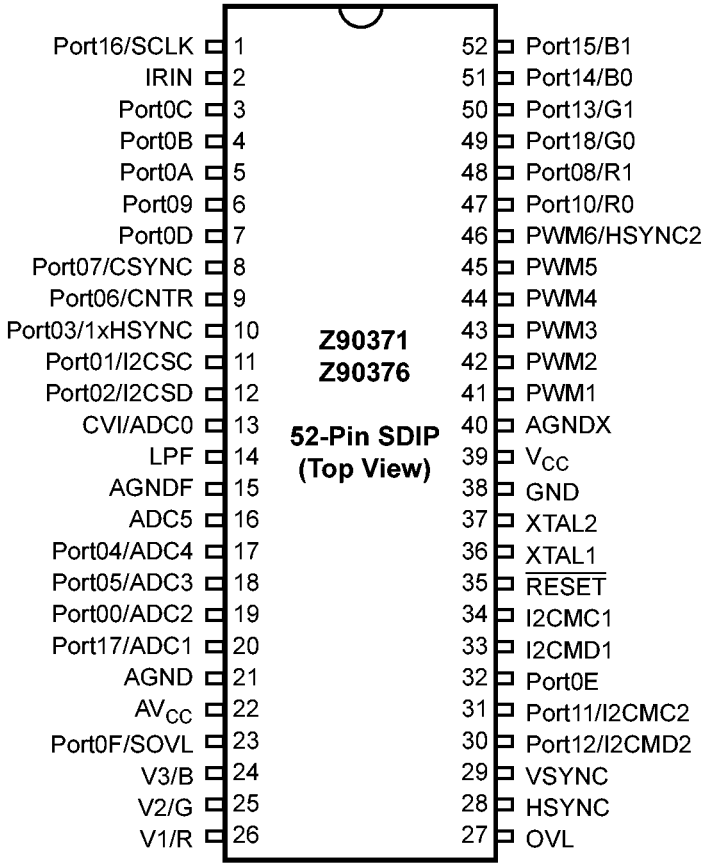


Figure 2. Z9037X Family Pin Diagram

FUNCTIONAL DESCRIPTION

The Z9037X Digital Television Controller is an application specific controller designed to provide complete audio and video control of television receivers and video recorders, and advanced on screen display facilities.

Applications

Figure 3 illustrates a typical application of the Z9037X Digital Television Controller as an embedded controller in a TV set. It provides the ability to decode closed-caption transmissions and display characters on the screen. Analog and digital control circuits can be manipulated. Keypad and infrared signals can be monitored directly. The Z9037X, for OSD generation, must receive vertical and horizontal synchronization signals.

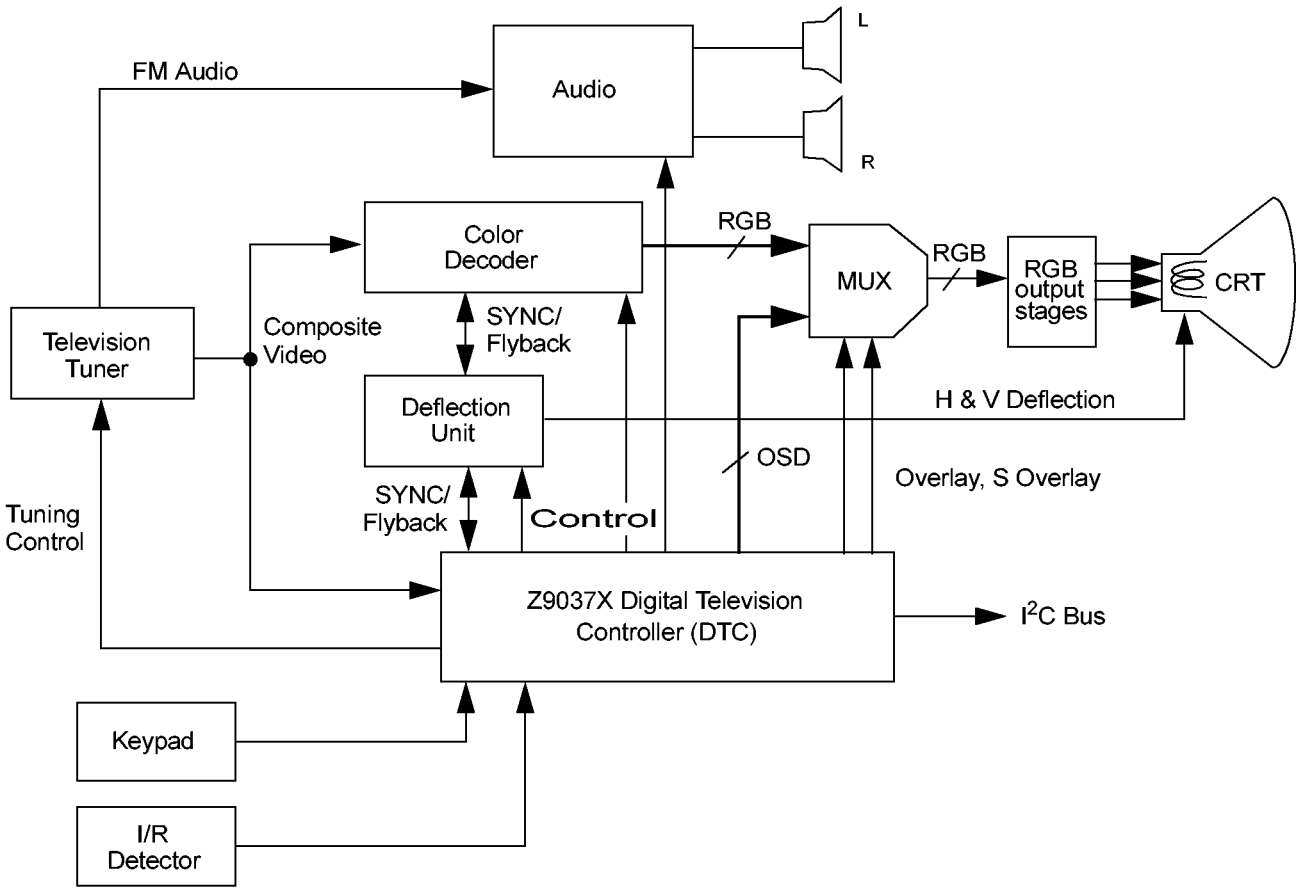


Figure 3. Z9037X Digital Television Controller System Application

In a typical system, normal transmission is received and demodulated. The CRT display is controlled by the signals received from the color decoder and deflection unit. In order to display characters generated by the Z9037X, a video multiplexor must be provided which enables the CRT display's RGB signals and synchronization to be controlled by the video outputs from the processor. When the controller must display a character on the screen, the multiplexor is switched, and the processor's video signals appear on the display.

The band-limited, A/C-coupled composite video signal is clamped internally to the negative reference voltage (REF–) during the back porch interval. It is then passed to the analog-to-digital converter through a 6:1 multiplexor. The digital signal is then decoded to extract the closed-caption text embedded in the video signal. The characters received are generated as video signals and are then passed to the display.

When a detectable composite video signal is received, the SYNC separator extracts the horizontal and vertical synchronization signals and passes them to the deflection module of the TV set. The FLYBACK signals from the deflection coils are fed back to the Z9037X. The controller uses these signals to align its video signals with those of the normal display. In the case where the composite video signal is not present, video synchronization is able to be provided by the controller. In this case, the SYNC signal pins are set to be outputs. The pins then feed to the deflection unit, which controls the display. The SYNC generators can be configured to provide either HSYNC and VSYNC, or H-FLYBACK and V-FLYBACK.

Analog functions such as volume and color controls can be controlled by the pulse width modulated outputs from the Z9037X. Other digital controls such as channel fine tuning can be controlled via the serial I^2C bus.

An infrared remote control receiver can be directly decoded through the capture register, and keypad input can be scanned by directly controlling I/O pins as keyscan ports.

The processor clock is provided by referencing an internal phase locked loop to an external 3.2768-kHz crystal oscillator. This oscillator enables EMI emissions from the clock circuitry to be minimized. The internal system clock frequency can be software selected to be 12.058 MHz in normal operation or 3.2768 kHz in low power consumption (SLEEP) mode (which is usually used in case of general system power failure). The Z9037X can also be placed in STOP mode, suspending processor clocking for power-down suspension of operation.

Program, display, and character graphics memory are on the chip, eliminating the requirement for any external memory components. Characters can be displayed as two or three times normal size. Smoothing and fringing circuits are provided to enhance display appearance.

Core Processor

The processor core is a high-performance DSP processor.

The powerful 12-MHz Z89C00 DSP processor core allows the user to control the on-board peripheral functions and registers using the standard processor instruction set. The Z9037X controller processor core is a Z89C00 high-performance 16-bit DSP processor optimized for data processing and transfer. 16-bit peripheral registers are programmed to control the operation of the peripheral devices. Four banks of 256 words each (total RAM in the processor core) can be used for video character sequence storage. Program and character graphics are stored in the PROM.

Note: The Z89C00 core used in Z9037X family devices is modified. The multiplier is disabled and is not accessible for the user, while X and Y registers of the multiplier are still available and can be used in software as general purpose registers.

Clocking Operation

The processor is able to operate from a number of clock sources.

- Primary Phase Locked Loop VCO source (PVCO)
- 3.2768-kHz oscillator clock (OSC)

In addition, the processor clock may be halted temporarily to allow clock selection or ROM accesses to be performed without disrupting normal operation of the processor.

An external crystal controls the internal 3.2768-kHz oscillator. The crystal is used as the clock reference for the internal 24-MHz Phase Locked Loop (PLL). The PLL provides the internal 12-MHz PVCO (primary VCO) clock for processor operation. SCLK is generated internally by dividing the frequency of an appropriate oscillator (PVCO) by 2. The frequency of the SCLK after POR is 12.058 MHz. In SLEEP mode, the controller uses the 3.2768-kHz clock for the SCLK to reduce power consumption. The processor can be suspended by placing it into STOP mode when main power is not available for minimal power consumption.

The SCLK signal can be brought out to the Port16 output pin under S/W control by setting a bit in the control register. The SVCO is used for display by the OSD only.

Read Only Memory (ROM)

The programmable ROM is designed to provide storage for both program memory (PROGROM) and character set graphic pixel arrays (CGROM). The address boundaries between these applications is dependent on the storage required for character graphics.

The program ROM section can, in theory, be accessed anywhere in the addressable ROM space; however, because CGROM usually starts at location 0000h, PROGROM will reside in the higher address locations. The maximum available ROM space for program memory depends on the ROM reserved for CGROM (for an application) and the ROM size of the device selected.

The size of memory used as CGROM depends on the number and resolution of characters stored in memory. An "n" represents the number of characters stored, ranging from 0 to 256. If characters are 16<symbols>× 18 pixels, then the upper region of memory starting at the 4K boundary is used for character storage. If not, that region can be used as program memory.

Table 3. ROM Organization

Memory	Program ROM	Hex Address
64K	int0 vector	%FFFF
	int1 vector	%FFFE
	int2 vector	%FFFD
	reset vector	%FFFC
up to 5K	CGROM program ROM	%1400
up to 4.5K	CGROM—Bank0, pixels 19, 20 or Bank1	%1200
4K	CGROM—Bank0, pixels 17, 18 or Bank1	%1000
up to 4K	CGROM program ROM	%10*n
0	CGROM—Bank0 (n characters) pixels 1–16	%0000

Random Access Memory (RAM)

RAM is organized in banks of 256 words consisting of 16 bits each. Bankl.0 is always accessible. Bank0.0 is mapped to other bank(s); only one gauge from 0.X is active through bit selection.

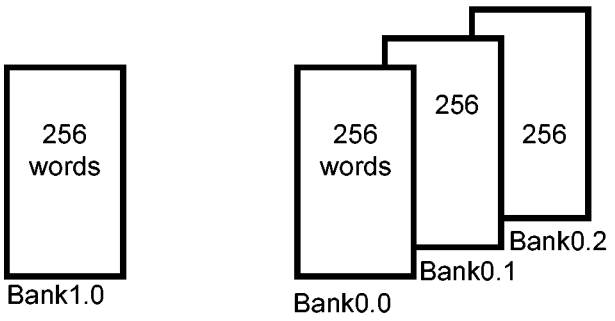


Figure 4. Random Access Memory (RAM)

External Registers

The C00 module is capable of directly accessing up to eight external registers using only the three external register address signals that are normally available. In this implementation, two user signals are combined with the register address signals to provide the ability to address four banks of eight registers each. The most speed critical registers are located together in bank 3. In this document, all external registers are referred to as follows:

RX(Y)<Z>,

where:

X is a register number within a register bank;
Y is a bank number; and
Z is a bit field number

The user can select a register by first setting the user bits to define the bank that the register is in and then specifying the address of the register on the external register address bus.

The external registers reside on the chip and are used to control the operation of all of the peripheral modules of the device. By reading or writing to the fields in the external registers, the user can interact with the peripheral devices of the chip.

The control is performed by ORing selected attributes from the Latched Attribute Register (value equal to R3(3)<8>). Attributes not selected are controlled by the Latched Attribute Register only.

Interrupt Control

The Z89C00 core exhibits three external interrupt signals that are used to provide interrupt signalling from the Z9037X peripheral modules to the core. There are four interrupt sources: horizontal sync (HSYNC), vertical sync (VSYNC), capture timer and external event (Port09). All interrupts are nonvectored. The capture timer and Port09 are multiplexed to the same interrupt.

Interrupt priorities are programmable. Each interrupt can be masked by setting fields in the external registers.

When the Z9037X receives an interrupt request from one of the interrupt sources, it directly executes the interrupt service routine for that source.

Timers

On-chip timers support IR captioning, real time clock, and watch-dog functions.

The capture timer is used to measure time between edges of the IR signal. This timer is programmable to measure timing from positive-to-positive, negative-to-negative, positive-to-negative, or negative-to-positive edges.

ON-SCREEN DISPLAY (OSD) (Continued)

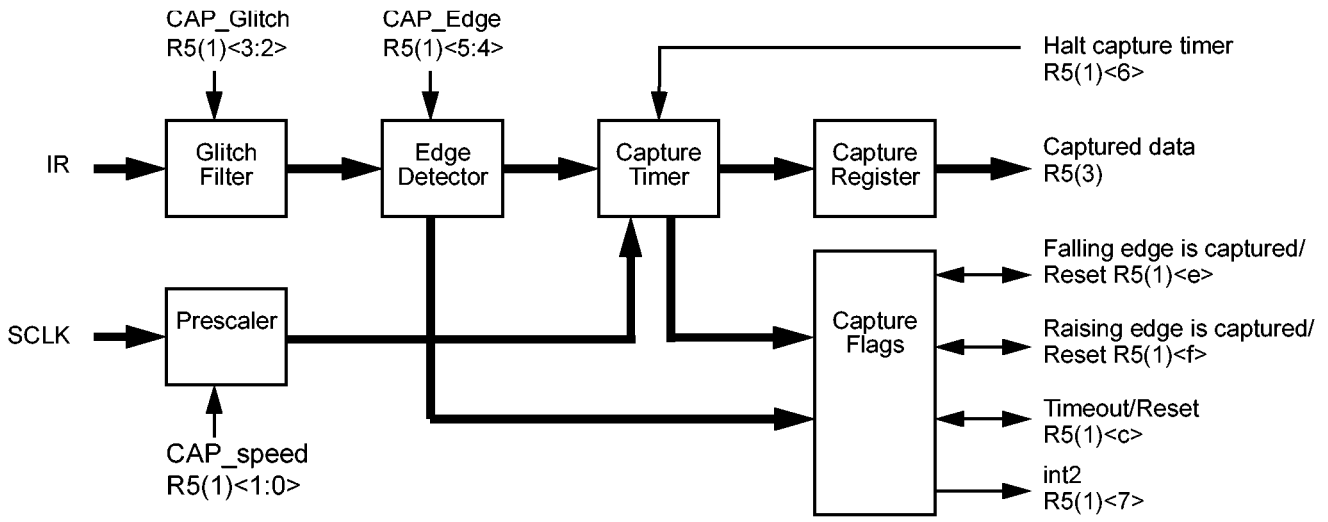


Figure 5. IR Capture Register Block Diagram

A clock timer, in real time, generates ticks every 1000, 250, 62.5 or 15.625ms.

A watch-dog timer is used in critical applications where external conditions like voltage spikes and/or noise might lock the CPU. In the latter case, the WDT will reset the CPU and restore its functionality.

ON-SCREEN DISPLAY (OSD)

The extensive character attributes can be controlled in two modes by the on screen display controller: character control mode for maximum display control flexibility and closed-caption mode for optimum display of closed-caption text.

The character control mode provides access to the full set of attribute controls. Each word of RAM specifies a single displayed character and basic character attributes, allowing the modification of attributes on a character-by-character basis. The insertion of control characters allows control of other character attributes.

The fully customizable character bank, available in multiples of 256 characters, can be displayed with a host of display attributes, including underlining, italics and blinking, eight foreground and background colors, character position offset delay, and background transparency. The 16-bit display character representation allows the modification of some key attributes on a character by character basis. A character's pixel array is stored as a 16, 18 or 20 word representation in Character Graphics ROM (CGROM). The ROM contents are referenced by a 16-bit word stored in video RAM (VRAM) defining the character type and its key attributes.

Additional hardware provides the capability to display two or three times the normal size of typical characters. The smoothing logic contained in the on screen display circuit improves the appearance of larger fonts. Fringing circuitry can be activated to improve the visibility of text.

RGB outputs provide the direct video signals, and a blanking output is provided to control the video multiplexor. RGB outputs are available in two modes: digital and analog. In digital mode, the output video signal corresponds to a primary colors palette. Analog mode supports 16 different palettes (8 programmable and 8 fixed) which can be chosen under software control (for more detail, see Additional Control Registers section, page 40. In case of an analog mode, each of the RGB outputs is generated by a 2-bit DA converter. The user can switch those 2-bit digital inputs of the DA converter to Port pins P10, P13, P14, P15, P18 and P08 under S/W control by setting a bit in the control register.

The dot clock and vertical line synchronization is normally obtained from H_FLYBACK and V_FLYBACK.

OSD is completely software-controlled. There is hardware support for optimum generation of the character based

OSD; however, the CPU can bypass it and access pixels and attributes directly. The block diagram of the OSD data flow is illustrated in Figure 6.

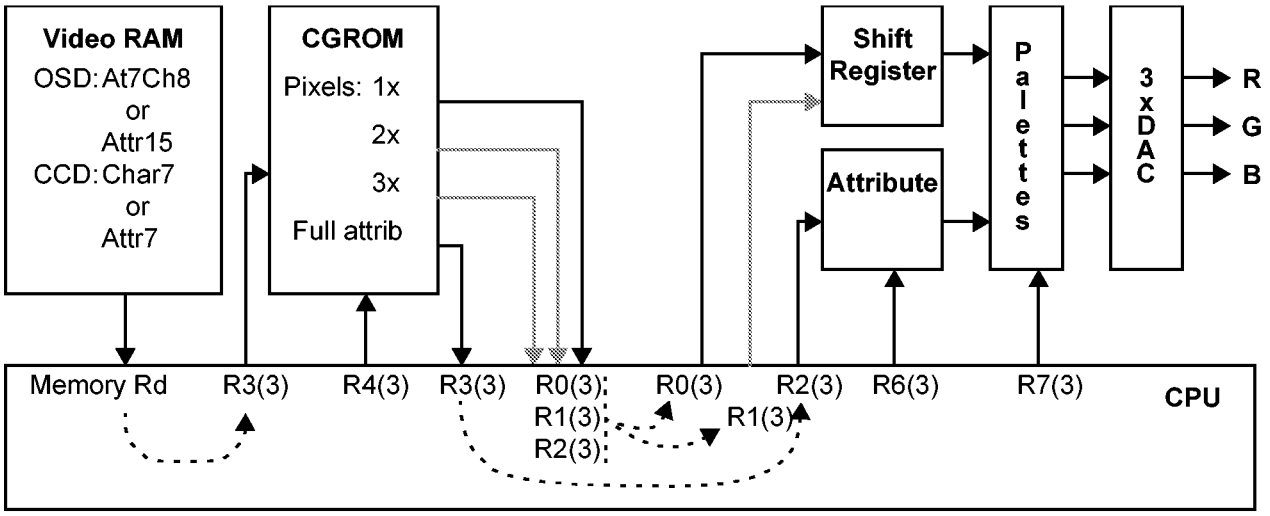


Figure 6. OSD Data Flow

Shadows/Fringing

Shadows/fringing if enabled are active on both transparent and nontransparent backgrounds. Two bits in the AttributeWR Register and AttributeRD registers (R2(3)<1:0> and R3(3)<1:0> control the shadow type selection as indicated below.

R2(3)<1:0>, R3(3)<1:0>	Function
00	No shadows
01	Left shadow
10	Right shadow
11	Both shadows (fringing)

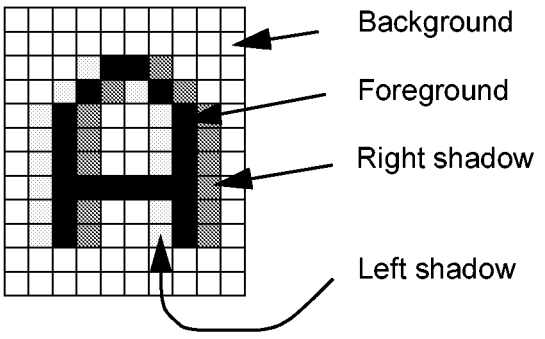


Figure 7. Table Settings

The smoothing attribute has been moved to R7(3)<5>.

The bit assignment in the Latched Attribute follows the bit assignment in R2(3).

The left and right shadow colors are independently controlled by R6(2)<d:b> and R6(2)<a:8>.

Note: The smoothing control bit R7(3)<5> must be set to a "1" in order to activate fringing.

ON-SCREEN DISPLAY (OSD) (Continued)

Semi-Transparency

Support for both semi-transparency (pin name: SOVL) and transparency (pin name: OVL) attributes have been implemented. The semi-transparency mode can be enabled through either latched or unlatched attributes. Latched attributes remain set until they are reset. Unlatched attributes remain set for only one character; therefore the attribute must be constantly refreshed on a character-by-character basis.

Activation. To activate the semi-transparency output, two bits must be properly set. Port 0F must be in output mode [R6(0)<f> = 0], and the SOVL/port0F control bit must be in SOVL mode [R3(1)<6> = 1].

Latched semi-transparency. The latched semi-transparency attribute is controlled by bit [R2(3)<6>].

Unlatched semi-transparency. The unlatched semi-transparency attribute is controlled by bit [R3(3)<8>]. This bit can take on 1 of 4 possible assignments depending on how it is setup in [R7(3)<7:6>]. The 4 assignments are underline, semi-transparency, blinking, and CGROM bank select.

Notes: Transparency and Semi-Transparency:

1. The semi-transparency signal (SOVL), when active, is only valid during the background color. During the foreground color SOVL is inactive. Therefore, characters do NOT take on a semi-transparent appearance (only the background does). This condition allows characters to be read without interference.

2. If both the transparency (background and foreground color are equal) and semi-transparency are activated, the transparency will take precedence over the semi-transparency. The OVL signal is High and the SOVL signal is Low.

Attribute_8 Assignment

Depending on R7(3)<7:6>, bit 8 of the Attribute_Data register, R3(3) (in character mode) can be assigned to control either "1st underline", "semi-transparency", "blinking", or "CGROM bank select":

Table 4. Attribute Assignment

R7(3)<7:6>	R3(3)<8>
00	1st underline (POR)
01	Semi-transparency
10	Blinking
11	CGROM bank1 select

CGROM (Character Generation ROM)

CGROM can be placed anywhere in the 64k ROM address space by setting the CGROM address offset register R7(2). This offset is added to the CGROM address before accessing ROM. By modifying the CGROM offset, several fonts can be accessed (limited by ROM size only). Upon reset, R7(2) = 0 (no offset) for backward compatibility is implemented with the existing software from Z903XX and Z893XX.

The required Character Graphics ROM size is dependent on the number of characters that are stored in memory. CGROM can be configured as multiple banks selectable by setting a CGROM offset register. Each bank provides up to 256 characters with 16x16-, 16x18-, or 16x20-pixel matrices.

Each character pixel array is represented as 16, 18 or 20 words of ROM storage. Each word represents 16 pixels. Pixel lines 1 to 16 are mapped sequentially to ROM addresses, referenced by the character pointer and a line number offset.

In 16x18 mode, pixel lines 17 and 18 are offset by 1000h (referenced to pixel line 1). In 16x20 mode, pixel lines 19 and 20 are offset by 1200h. Initially, if the offset of a bank is 0, then that bank is in 16x18 mode. This bank overlaps the first 32 characters of the next bank. If the first bank is in 16x20 mode, it overlaps the first 64 characters of the next bank. Because the first character in each bank should be a space character, it is recommended that the first bank characters be defined with a 16x16 matrix. If the application requires the first bank characters to be in 16x18 or 16x20 pixel format, the first 32 (64 for 16x20) characters of the next bank should be sacrificed. These characters should not be used, because lines 17 and 18 (19 and 20 for 16x20) of the first bank characters are mapped in their addresses. Also, the first 8 (16 for 16x20) characters of the first bank should not have any active pixels in lines 17 and 18 (and 19 and 20 for 16x20) in order to have a blank first (space) character in the next bank.

If only one CGROM is used, there is no limitation on character definitions.

The contents of the R0(3), R1(3), and R2(3) registers will contain a sequence of bits that represent whether the pixels on the pixel line currently being accessed for that character are on or off. This representation can be modified by the character multiplier to be two or three times normal character size. By duplicating each bit in the word and expanding the representation to two or three of the character multiplier registers, this condition is possible.

CGROM Relocation

CGROM can be placed anywhere in the 64k ROM address space by setting the CGROM address offset register R7(2). This offset is added to the CGROM address before accessing the ROM. By modifying the CGROM offset, several fonts can be accessed (limited by ROM size only). Upon reset, R7(2) = 0 (no offset), making the register backward-compatible with existing software.

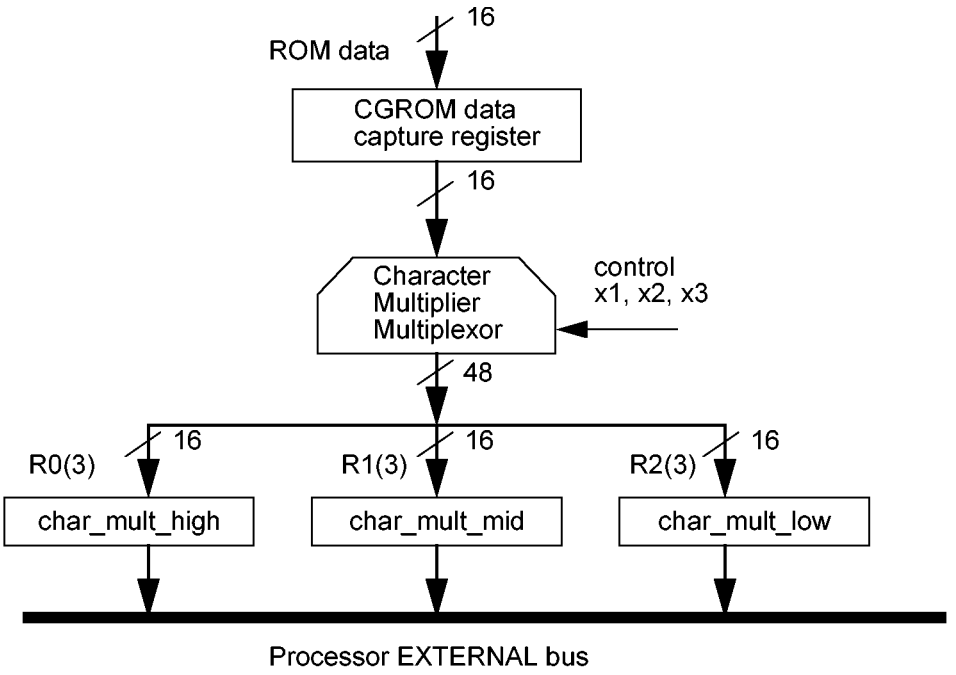


Figure 8. Character Multiplier

The design is based on the Z9035X/Z9037X with the addition of a line buffer. The latter one is organized as two independent memory arrays each capable of storing one video line. While one buffer fills with pixels at "normal" speed (12-MHz pixel rate), the other one displays previously stored pixels at twice the "normal" speed (24 MHz). Because filling the buffer takes twice as long as displaying, every line must either be displayed twice (referred to as "fast progressive mode") or be interleaved with a black line ("fast interlaced mode").

Memory Buffer Size Calculation

The current implementation of the Z9037X exists in two arrays of 1024 bytes each. The minimum size of the buffers depends on the OSD size. The current API requires 512 pixels (though some custom software may require more—up to 640 pixels).

Table 5. CGROM Offset Registers

Register Field	Bit Position	R	W	Data	Description
CGoffset	fedcba9876543210	R	W	xxxx	CGROM offset–POR=0000

ON-SCREEN DISPLAY (OSD) (Continued)

Character Size Multiplier Multiplexor

The character size multiplier multiplexor can be controlled to double or triple the size of the pixel data presented to it from the CGROM capture register. It does not perform a numerical multiplication. The bits of the word contained in the capture register are duplicated to enlarge the character as it would be displayed horizontally on the screen. A model of the operation of the character multiplier multiplexor is indicated in Table 6.

Table 6. Character Size Multiplier Format

capture register contents	char_mult_high	char_mult_mid	char_mult_low
x1 operation	abcdefghijklmnop		
x2 operation	aabbccddeeffgghh	iijjkkllmmnnoopp	
x3 operation	aaabbbcccdddeeef	ffggghhhiiijjjkk	klllmmmnnnoooppp

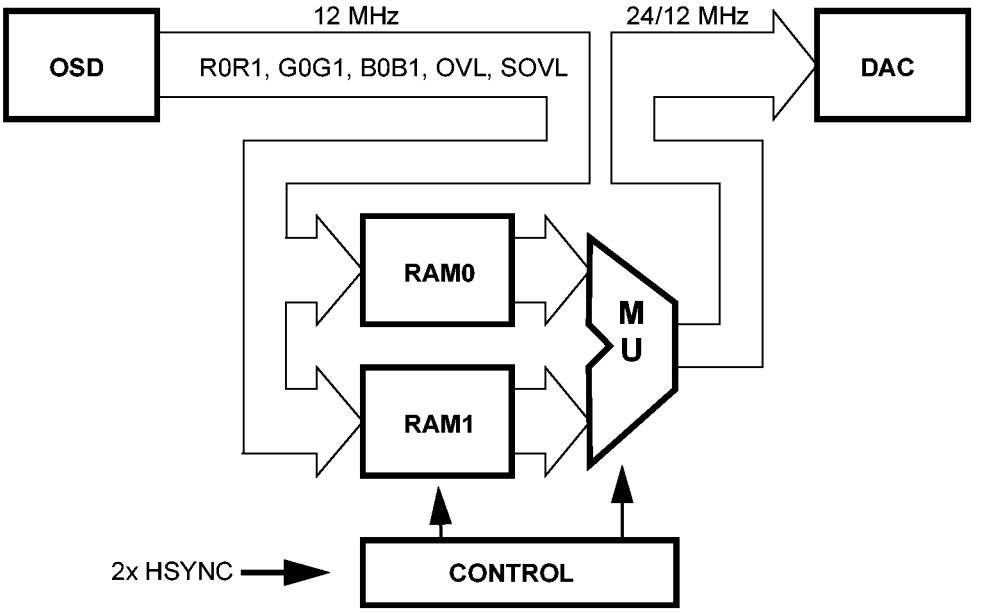


Figure 9. Display RAM

Fast Progressive Mode Operation

In fast progressive mode, every OSD line is displayed twice. The refresh rate of the OSD stays the same as the refresh rate of the video signal. The effective vertical resolution of the OSD reduces by a factor of two. This mode works for a progressive signal only.

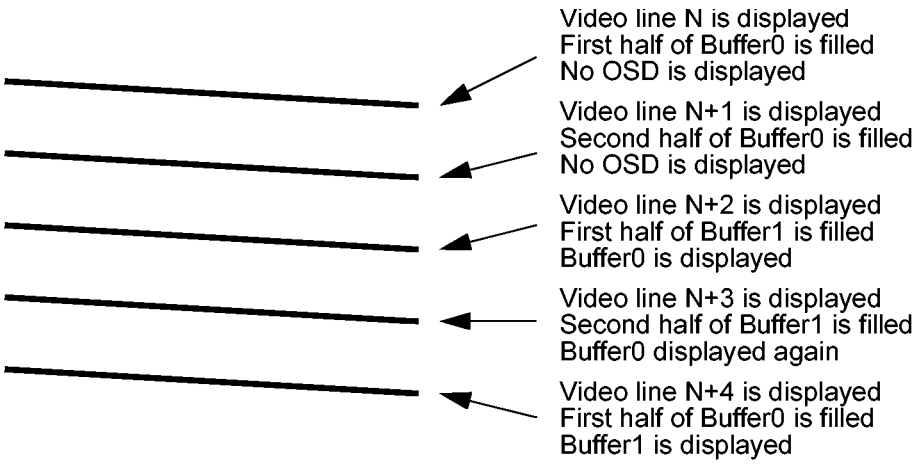


Figure 10. Fast Progressive Mode

Fast Interlaced Mode Operation

In fast interlaced mode, every OSD line is displayed one time, followed by a black line. The field black line is displayed first, followed by an OSD line. The refresh rate of the OSD is less than twice the refresh rate of the video signal (the effective vertical resolution of the OSD does not reduce). The OSD brightness decrease must also be compensated. This mode works for both a progressive and a double-scan signal. In the case of double-scan, there are four interlaced fields of OSD.

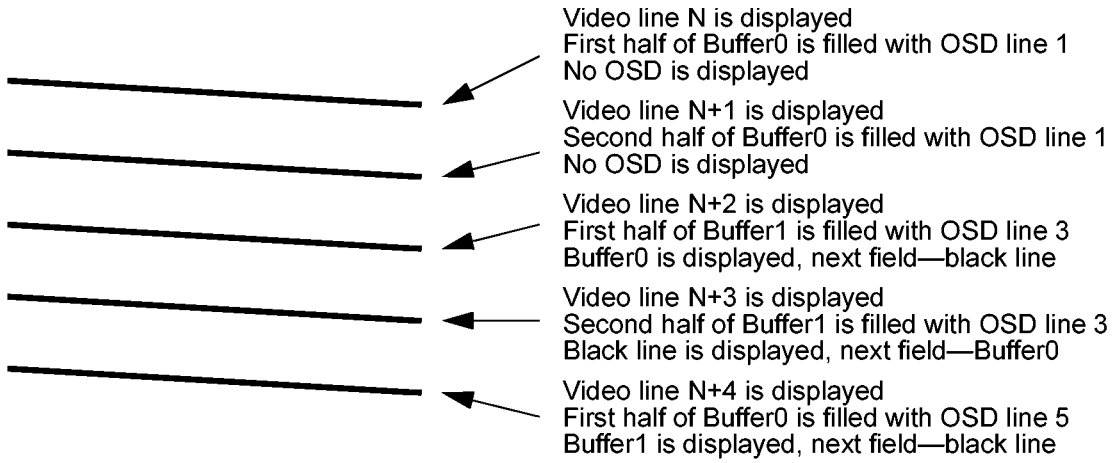


Figure 11. Fast Interlaced Mode

Mode selection is controlled by R1(1)<3> ("0"—progressive, "1"—interlaced).

Every field hardware should be initialized by writing a "1" into R1(1)<5> one time per every VSYNC.

Interleaving is performed by writing to "1/0" R1(1)<4> to select BLACK/OSD line to be displayed first. This execution must be performed one time per every VSYNC.

In order to get in sync with a "normal" (1x) HSYNC, a "skip next 2x HSYNC" function is implemented. Writing a "1" to R1(1)<6> results in skipping one HSYNC pulse. This action is recommended upon power-up and after a channel-switch. If 1xHSYNC is available externally, the data can feed in through the Port03 pin. R1(1)<7> controls the source of 1xHSYNC. Port03 should be assigned as an input.

Clock switching should always be disabled (R6(1)<4> = 1).

Horizontal position adjustment R6(1)<3:0> should be set to "F". Actual adjustment should be performed by R1(1)<c:7>.

OSD in internal HSYNC/VSYNC mode is supported only for standard interlaced mode.

If the OSD disable bit R3(1)<5> is set to "0", both OSD and line buffers are shut down to reduce EMI when no OSD is displayed.

If R1(1)<2> is set to "1", RGB output current is doubled.

Table 7. R1(1) Speed Control Register

Reg field	Bit position	R	W	Data	Description	Note
Reserved	f---------------				reserved	
	-e--------------	R	W	1	Standard interlaced mode (single scan mode)	
				0	Double-scan mode–POR	
H_SHIFT	--dcba98--------	R	W	%D	shift right in 4 pixels increment–POR = 0	
1xHSYNC	--------7-------	R	W	1	1xHSYNC is connected to Port03	
				0	1xHSYNC is 2xHSYNC/2–POR	
Skip_HSYNC	---------6------	N/A	W	1	Skip next HSYNC	
				0	Do not skip next HSYNC	
Frame_start	----------5-----	N/A	W	1	Field start initialization	1
				0	No effect	
OSD_black	-----------4----	R	W	1	next output line is OSD	2
				0	next output line is black	
Line_buffer_mode	------------3---	R	W	1	interlaced (OSD/black)	
				0	progressive (OSD/OSD)–POR	
2x_RGB	-------------2--	R	W	1	Double RGB output	
				0	Normal RGB output–POR	
Fast_enable	--------------1-	R	W	1	PVCO/SVCO enabled	
				0	PVCO/SVCO disabled–POR	
Fast_slow	---------------0	R	W	1	SCLK is 12.058 MHz	
				0	SCLK is 32.768 KHz–POR	

Notes:
1. Frame_start should be set to "1" in the beginning of every field.
2. OSD_black controls interlacing in interlaced mode.

Cursor

The cursor is implemented as a one-line pixel buffer. The cursor buffer is loaded via the DMA on every line where the cursor is to be displayed (no software support is required). Horizontal size is programmable at 16, 32 or 48 pixels wide, and vertical size is programmable from 1 to 63 lines per field. The color depth is 2 bits per pixel—3 programmable colors and the transparency. Depending on R1(0)<d>, the cursor's colors can be selected either from a current palette (R1(0)<d> = 0) or from Palette #6 (refer to Table 41) (R1(0)<d> = 1). The cursor image is stored in ROM as a bitmap. The number of different cursors is limited by ROM size only.

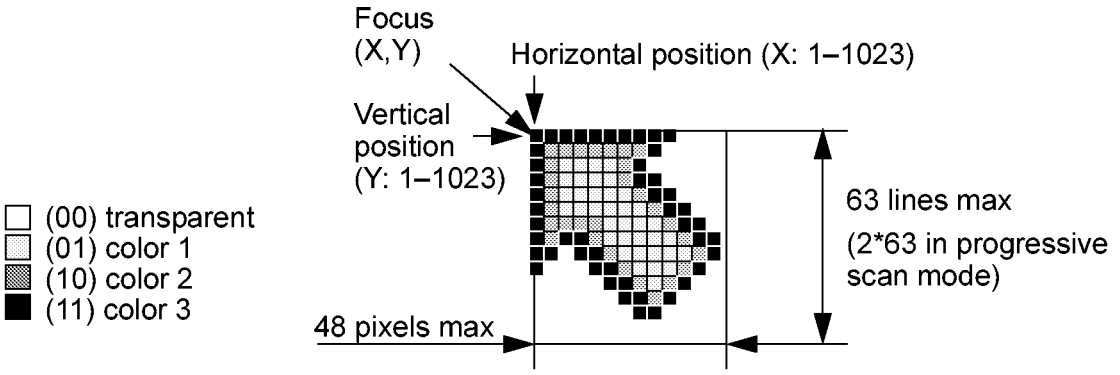


Figure 12. Cursor

Cursor positioning is performed by initializing cursor parameters in the beginning of every field.

Initialization is performed by first setting the Cursor_Info_Load bit R7(3)<4> to "1", followed by writing sequentially to the R3(3) 16-bit parameters—COLOR, HPARAM, VPARAM and CADDR—respectively.

ON-SCREEN DISPLAY (OSD) (Continued)

```
Example: LD   SR,%#60          ; select RegBank3
         OR   EXT7,#%0010      ; enable
         Cursor_Info_Load
         LD   EXT3,#(3*64 + 7*8 + 2);  load  CCOLOR:
         color3 = 3, color2 = 7, color1 = 2
         LD   EXT3,#(2*1024 + 120);  load  HPARAM:
         hsize = 2 (32 pixels), hpos = 120
         LD   EXT3,#(28*1024 + 55);  load  VPARAM:
         vsize = 28, vpos = 55
         LD   EXT3,#%6000      ; load CADDR—cursor
         bitmap address
         AND EXT7,#%FFEF       ; disable
         Cursor_Info_Load, ready for OSD
```

Table 8. Cursor Parameters

Parameter	Reg field	Bit position	Data	Description
CADDR	CADDR	fedcba9876543210	%DDDD	Cursor bitmap address (pointer to cursor bitmap in ROM)
VPARAM	VSIZE	fedcba----------	1–63	Vertical size (lines in one field)
	VPOS	------9876543210	1–1023	Vertical position (lines in one field)
HPARAM	n/a	fedc------------	n/a	Reserved
	HSIZE	----ba----------	00 01 10 11	No cursor 16 pixels wide 32 pixels wide 48 pixels wide
	HPOS	------9876543210	1–1023	Horizontal position (pixels from trailing edge of HSYNC)
CCOLOR	n/a	fedcba9---------	n/a	Reserved
	Color3	-------876------	0–7	Cursor Color 2 assignment
	Color2	----------543---	0–7	Cursor Color 1 assignment
	Color1	------------210	0–7	Cursor Color 0 assignment

The cursor buffer is loaded from ROM at the leading edge of HSYNC wherever this horizontal line should have a cursor. This process halts the CPU for 3/5/7 cycles depending on the cursor's horizontal size. The cursor bitmap address pointer (CADDR) is incremented automatically.

Though the cursor can be displayed anywhere on the screen, it is recommended to limit the cursor to the OSD area. Outside of the OSD area, the cursor may jitter or become distorted.

The cursor bitmap is organized as pixel data sequentially placed in the ROM. The data format is described below.

For the interlaced mode, even and odd cursor bitmaps should be separately defined. Proper selection is performed during the cursor's initialization at the beginning of every field.

MEMORY ALLOCATION FOR CURSOR'S BITMAP

16 Pixels Wide Mode

```
AddrN:      L0_P15_B0,      L0_P14_B0,    L0_P13_B0, ... ,     L0_P1_B0,   L0_P0_B0
AddrN+1:    L0_P15_B1,      L0_P14_B1,    L0_P13_B1, ... ,     L0_P1_B1,   L0_P0_B1
AddrN+2:    L1_P15_B0,      L1_P14_B0,    L1_P13_B0, ... ,     L1_P1_B0,   L1_P0_B0
AddrN+3:    L1_P15_B1,      L1_P14_B1,    L1_P13_B1, ... ,     L1_P1_B1,   L1_P0_B1
.................................................
AddrN+2n:   Ln_P15_B0,      Ln_P14_B0,    Ln_P13_B0, ... ,     Ln_P1_B0,   Ln_P0_B0
AddrN+2n+1:Ln_P15_B1,       Ln_P14_B1,    Ln_P13_B1, ... ,     Ln_P1_B1,   Ln_P0_B1
```

32 Pixels Wide Mode

```
AddrN:      L0_P31_B0,      L0_P30_B0,    L0_P29_B0, ... ,     L0_P17_B0,  L0_P16_B0
AddrN+1:    L0_P31_B1,      L0_P30_B1,    L0_P29_B1, ... ,     L0_P17_B1,  L0_P16_B1
AddrN+2:    L0_P15_B0,      L0_P14_B0,    L0_P13_B0, ... ,     L0_P1_B0,   L0_P0_B0
AddrN+3:    L0_P15_B1,      L0_P14_B1,    L0_P13_B1, ... ,     L0_P1_B1,   L0_P0_B1
AddrN+4:    L0_P31_B0,      L0_P30_B0,    L0_P29_B0, ... ,     L0_P17_B0,  L0_P16_B0
AddrN+5:    L0_P31_B1,      L0_P30_B1,    L0_P29_B1, ... ,     L0_P17_B1,  L0_P16_B1
.................................................
AddrN+4n:   Ln_P31_B0,      Ln_P30_B0,    Ln_P29_B0, ... ,     Ln_P17_B0,  Ln_P16_B0
AddrN+4n+1:Ln_P31_B1,       Ln_P30_B1,    Ln_P29_B1, ... ,     Ln_P17_B1,  Ln_P16_B1
AddrN+4n+2:Ln_P15_B0,       Ln_P14_B0,    Ln_P13_B0, ... ,     Ln_P1_B0,   Ln_P0_B0
AddrN+4n+3:Ln_P15_B1,       Ln_P14_B1,    Ln_P13_B1, ... ,     Ln_P1_B1,   Ln_P0_B1
```

48 Pixels Wide Mode

```
AddrN:      L0_P47_B0,      L0_P46_B0,    L0_P45_B0, ... ,     L0_P13_B0,  L0_P32_B0
AddrN+1:    L0_P47_B1,      L0_P46_B1,    L0_P45_B1, ... ,     L0_P33_B1,  L0_P32_B1
AddrN+2:    L0_P31_B0,      L0_P30_B0,    L0_P29_B0, ... ,     L0_P17_B0,  L0_P16_B0
AddrN+3:    L0_P31_B1,      L0_P30_B1,    L0_P29_B1, ... ,     L0_P17_B1,  L0_P16_B1
AddrN+4:    L0_P15_B0,      L0_P14_B0,    L0_P13_B0, ... ,     L0_P1_B0,   L0_P0_B0
AddrN+5:    L0_P15_B1,      L0_P14_B1,    L0_P13_B1, ... ,     L0_P1_B1,   L0_P0_B1
AddrN+6:    L0_P47_B0,      L0_P46_B0,    L0_P45_B0, ... ,     L0_P33_B0,  L0_P32_B0
AddrN+7:    L0_P47_B1,      L0_P46_B1,    L0_P45_B1, ... ,     L0_P33_B1,  L0_P32_B1
.................................................
AddrN+6n:   Ln_P47_B0,      Ln_P46_B0,    Ln_P45_B0, ... ,     Ln_P33_B0,  Ln_P32_B0
AddrN+6n+1:Ln_P47_B1,       Ln_P46_B1,    Ln_P45_B1, ... ,     Ln_P33_B1,  Ln_P32_B1
AddrN+6n+2:Ln_P31_B0,       Ln_P30_B0,    Ln_P29_B0, ... ,     Ln_P17_B0,  Ln_P16_B0
AddrN+6n+3:Ln_P31_B1,       Ln_P30_B1,    Ln_P29_B1, ... ,     Ln_P17_B1,  Ln_P16_B1
AddrN+6n+4:Ln_P15_B0,       Ln_P14_B0,    Ln_P13_B0, ... ,     Ln_P1_B0,   Ln_P0_B0
AddrN+6n+5:Ln_P15_B1,       Ln_P14_B1,    Ln_P13_B1, ... ,     Ln_P1_B1,   Ln_P0_B1
```

Where:

Lx_Py_Bz = line X, pixel Y, bit Z;

Line 0 = first (top) cursor's line;

Pixel 0 = first (left) cursor's pixel

Bit 1, Bit 0 = most and least significant bit of the cursor's color defined as:

00 = transparent

= 01 = Color 1

= 10 = Color 2

= 11 = Color 3

Tuner Control

Serial interfacing with the television tuner is provided via the industry standard I^2C port.

Video and Sound Attribute Control

Basic receiver functions (such as color and volume) can be directly controlled by six 6-bit pulse-width modulated ports and one 14-bit pulse-width modulated port.

One 14-bit and up to six 6-bit pulse-width modulated outputs are available to provide PWM control of analog signal levels such as volume or color.

Vertical Blank Interval Data Capture

Closed-caption text can be decoded directly from the composite video signal with the assistance of the processor's digital signal processing capabilities and displays on the screen. The character representation in this mode allows for simple attribute control through the insertion of control characters, with each word of RAM specifying two displayed characters.

The 4-bit flash A/D converter, with proper clamping, provides the ability to directly receive the composite video signal and process the closed-caption text embedded in the signal. Signal processing can be applied directly to the signal to improve decoder performance.

ADC and Clamp Circuit

This function employs a 4-bit resolution, flash A to D converter. The six-to-one analog input multiplexor and conversion start circuits are controlled by the user program. The 4-bit conversion result is available to be read by the CPU at the end of each conversion.

One input channel (ADC0) is dedicated for quantizing VBI (vertical blank interval) data for subsequent digital signal processing. Another channel, ADC5, is typically used for VSYNC separation from the composite TV signal. These channels (ADC0 and ADC5) have a special video clamp circuit that provides DC restoration of the composite video input signal. Typical VBI applications include Line 21 Closed Caption, Electronic Data Services, and StarSight Telecast. The range of ADC0 and ADC5 is from 1.5 to 2.0 V.

The four remaining channels of ADC (ADC1, ADC2, ADC3, and ADC4) are general purpose. They are typically used for implementation of tuner automatic frequency control and analog key entry. The range of ADC1–ADC4 is from 0 to 5.0 V.

In the Z9037X, the range of ADCs is programmable from 1.5 to 2.0V or 0 to 5V.

The 4-bit ADC implemented in the Z9037X features six multiplexed inputs.

The allowed range of the input signals is different for different ADC inputs according to the Table 9.

Table 9. ADC Inputs Typical Range

Input	Range (V)	Clamping	Typical application
CVI/ADC0	1.5–2.0	Yes (Ref–)	CCD sampling input
ADC1/P17	0–5.0	No	AFC input
ADC2/P00	0–5.0	No	Key scanning input
ADC3/P05	0–5.0	No	Key scanning input
ADC4/P04	0–5.0	No	Key scanning input
ADC5	1.5–2.0	Yes (Ref+)	VSYNC decoder sampling input

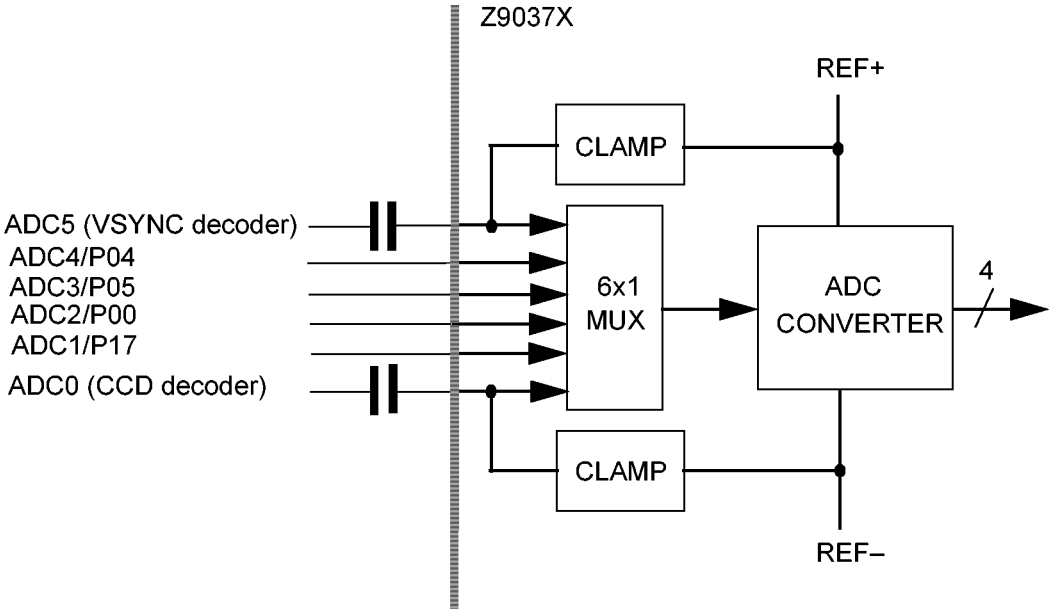


Figure 13. ADC Block Diagram

Internally generated reference voltages define the maximum range of the input signal of the ADC. Nominal values of Ref+ = 2.0 V; Ref– = 1.5 V @ V_{CC} = 5.0 V. For different values of V_{CC}, the reference voltages should be prorated as:

$$Ref+ = 0.4 * V_{CC}; \quad Ref- = 0.3 * V_{CC}$$

The maximum sampling rate of the ADC converter is 3 MHz. It takes 4 SCLK cycles for the valid data at the output of the ADC to become available. This matter should be taken into consideration especially if the application is utilizing a single shot mode.

The ADC converter exhibits guaranteed monotonous conversion characteristics with a nonlinearity of less than 0.5 LSB. ADC0 and ADC5, which exhibit a range of 0.5V (from 1.5V to 2.0V), are directly multiplexed to the input of the ADC. The remaining ADC inputs (ranging from 0V to 5V) use AGND and AV_{CC} voltage as an reference.

ADC Data Packing

Up to four 4-bit ADC data samples can be packed into one 16-bit word without software overhead. If R4(1)<9> = 1, every reading of R4(1) will return the result, Where High 12 bits are the three previous ADC samples, and the Low 4 bits are the current one:

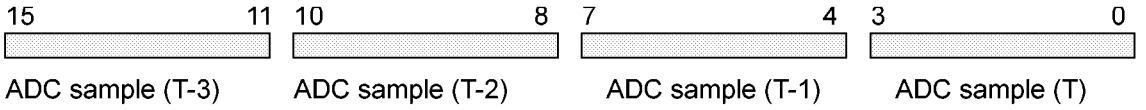


Figure 14. ADS Data Packing

MEMORY ALLOCATION FOR CURSOR'S BITMAP (Continued)

Example: NOPs between ADC accesses are omitted.

```
LD   SR,%#20    ; select RegBank1
LD   A,EXT4     ; turn "ADC data packing" mode on
OR   A, #%0200  ;
LD   EXT4, A    ;
LD   A, EXT4    ; read first ADC sample, A = %0005
LD   A, EXT4    ; read second ADC sample, A = %005E
LD   A, EXT4    ; read third ADC sample, A = %05E7
LD   A, EXT4    ; read forth ADC sample, A= %5E74
LD   A, EXT4    ; read fifth ADC sample, first sample is thrown away, A = %E741
```

Example:

```
LD   SR,#%20          ; Select RegBank1
LD   A,EXT4           ; turn "hardware supported shift" mode on
AND A, #%9FFF         ;
OR   A, #%4000        ;
LD   EXT4, A          ; select "4-bit right rotate"
LD   A, #%3ED7        ; load A = %3ED7
LD   %1FE, A          ; write A to the RAM
LD   A, %1FE          ; A = %73ED
LDA,EXT4; turn "hardware supported rotate" mode on
OR   A,#%6000         ;
LD   EXT4, A          ; select "byte swap"
LD   A, %1FE          ; A = %D73E
```

Capture Function

The capture function is intended for Infrared Remote Control data capture. It employs a capture register that holds the time value from one transition of IR data to the next.

Software can periodically check the capture status and read the value if a new capture occurs. Subsequent decoding and command passing of the received IR signal is under software control.

Hardware Accelerated 4-Bit and 8-Bit Shifts

Hardware accelerated byte and nibble shifts significantly reduce software overhead. Shifts are implemented by assigning one particular RAM location (%1FE) a special meaning. Depending on the R4(1)<e:d> settings data read from this address is either unmodified, rotated 4 bits left, 4 bits right or byte swapped.

Table 10. R4(1)<e:d> Settings

R4(1)<e:d>	Function
00	Direct (unmodified)–POR
01	4-bit left rotate
10	4-bit right rotate
11	Byte swap

Pulse Width Modulators (PWMs)

Pulse Width Modulation is used in conjunction with external low-pass filters to perform digital to analog conversion. Six PWMs, (8-bit resolution each) find application in generating signals for the control of video and sound attributes. One 14-bit PWM (PWM9) may be used with an external circuit to generate controlling voltage for voltage synthesis tuners. In case of a chassis employing a frequency synthesis tuner, these PWMs may also control video or sound attributes.

Each PWM circuit features a data register whose contents are set under program control. The data in the register determines the ratio of PWM High to PWM Low time. PWM data registers are not initialized upon reset. In order to eliminate a potential glitch on a PWM output, it is recommended to initialize PWM data registers before enabling the VCOs.

I/O Ports

User control can be monitored either through the keypad scanning port, or the 16-bit remote control capture register.

Two input/output port blocks are available for general purpose digital I/O application. Each port bit is programmable to be either input or output. To conserve the device pin count, some port pins are mapped to provide I/O to the ADC converter block and I^2C interface block.

The 25 configurable I/O pins are general purpose pins that can be utilized to provide functions such as serial data I/O, LED control, key scanning, power control and monitoring, and I^2C serial data communications.

I²C Interface[1]

There are two completely independent H/W modules which support a standard I²C bus protocol according to the I²C bus specification published by Phillips in 1992, entitled *I²C Peripherals for Microcontrollers Data Handbook*. The first module, referred to as a "master", can be configured for fast (400 kHz) or slow (100 kHz) bit rates and can be used in applications with a single master. The second module, referred to as a "slave", supports a 7-bit addressing format with both fast and slow bit rates. The Z9037X adds two additional nonstandard bit rates (50kHz and 10kHz) and an additional multiplexed master port that is controlled by the I²CM_mux control bit.

[1]Philips Standard Serial Interface.

Table 11. Master I²C Bus Bit Rates

Mode	I²C mode	Bit rate	Actual bit rate
LO/Slow	—	0–10kHz	10kHz
HI/Slow	—	0–50kHz	44kHz
LO/Fast	Slow	0–100kHz	91kHz
HI/Fast	Fast	0–400kHz	334kHz

In order to suppress possible glitches on both data (SDA) and clock (SCL) lines, digital filters (with a time constant equal to $3T_{SCLK}$ = 250 ns) are implemented on all inputs of the I²C bus interface.

If the master or slave I²C interface is enabled, the correspondent I/Os (Port01 and Port02 for the slave, Port11 and Port12 for the master) must be assigned as outputs.

Though both master and slave modules operate independently and can be used for simultaneous communication via two I²C buses, from the software viewpoint they still share one control register. The software activates I²C modules by writing appropriate commands into the control register. In order to control the I²C bus interface, the control register R3(0) toggle bit <c> should point to a desired interface (Master or Slave).

M_disable (S_disable) bits allow either of the I²C interfaces (Master or Slave) to be disabled and not to interfere with any activity of the Port pins. Upon POR, both of the I²C interfaces are enabled. In order to use the I²C interface, the corresponding Port pin (which is multiplexed with the I²C Data and Clock) should be configured as an input, while M_disable (S_disable) bits should be reset to "0".

MEMORY ALLOCATION FOR CURSOR'S BITMAP (Continued)

Table 12. Master I^2C Bus Interface Commands

Command	Notes/Function
0 0 0	This command sends a start bit, followed by an address byte specified in the "data" field (bits <7:0>), then fetches an acknowledgment in bit <0>. This command is used to initialize communication, and generates 9 SCL cycles.
0 0 1	This command sends one byte of data specified in the "data" field (bits <7:0>), then fetches an acknowledgment in bit <0>. This command is used in a WRITE frame, and generates 9 SCL cycles.
0 1 0	This command sends bit <7> as an acknowledgment (ACK = 0, NAK = 1), then receives a data byte. This command is used in a READ frame when the next data byte is expected, and generates 9 SCL cycles. Received data is read in the "data" field (bits <7:0>).
0 1 1	This command sends bit <7> as an acknowledgment (ACK = 0, NAK = 1). This command is used in a READ frame to terminate data transfer, and generates one SCL cycle.
1 0 0 1 0 1	A NULL operation. This command must be used together with a "RESET" bit <b> and/or "TOGGLE" bit <c>. If "RESET" and/or "TOGGLE" bits are used in conjunction with any other command, the functionality of the I^2C interface logic is not guaranteed.
1 1 0	This command receives one data byte. This command is used in a READ frame in order to receive the first data byte after the address byte is transmitted, and generates 8 SCL cycles.
1 1 1	This command sends a stop bit, and generates one SCL cycle.

Table 13. Slave I^2C Bus Interface Commands

Command	Notes/Function
0 0 0	Reserved—cannot be used.
0 0 1	This command sends a bit <7> as an acknowledgment (ACK = 0 only), then receives one data byte. This command is used in a WRITE frame. Requires 9 SCL cycles. Received data is read in "data" field (bits <7:0>).
0 1 0	This command sends one byte of data specified in "data" field (bits <7:0>), then fetches an acknowledgment in bit <0>. This command is used in a READ frame, and requires 9 SCL cycles.
0 1 1	Reserved. Can not be used.
1 0 0 1 0 1	A NULL operation. This command must be used together with a "RESET" bit <b> and/or "TOGGLE" bit <c>. If "RESET" and/or "TOGGLE" bits are used in conjunction with any other command, the functionality of the I^2C interface logic is not guaranteed.
1 1 0	This command sends a bit <7> as a *not acknowledgment* (NAK = 1 only) in a WRITE or READ frame. This command is used to terminate the I^2C communication, and requires one SCL cycle. The "Sulfonamide" bit <a> is automatically reset upon a "busy" bit <9> going Low. This command sends a bit <7> as an acknowledgment (ACK = 0 only) in a READ frame, and requires one SCL cycle. The Send data command (010) must be executed next. This command is used to acknowledge an address byte in a READ frame.
1 1 1	Reserved—cannot be used.

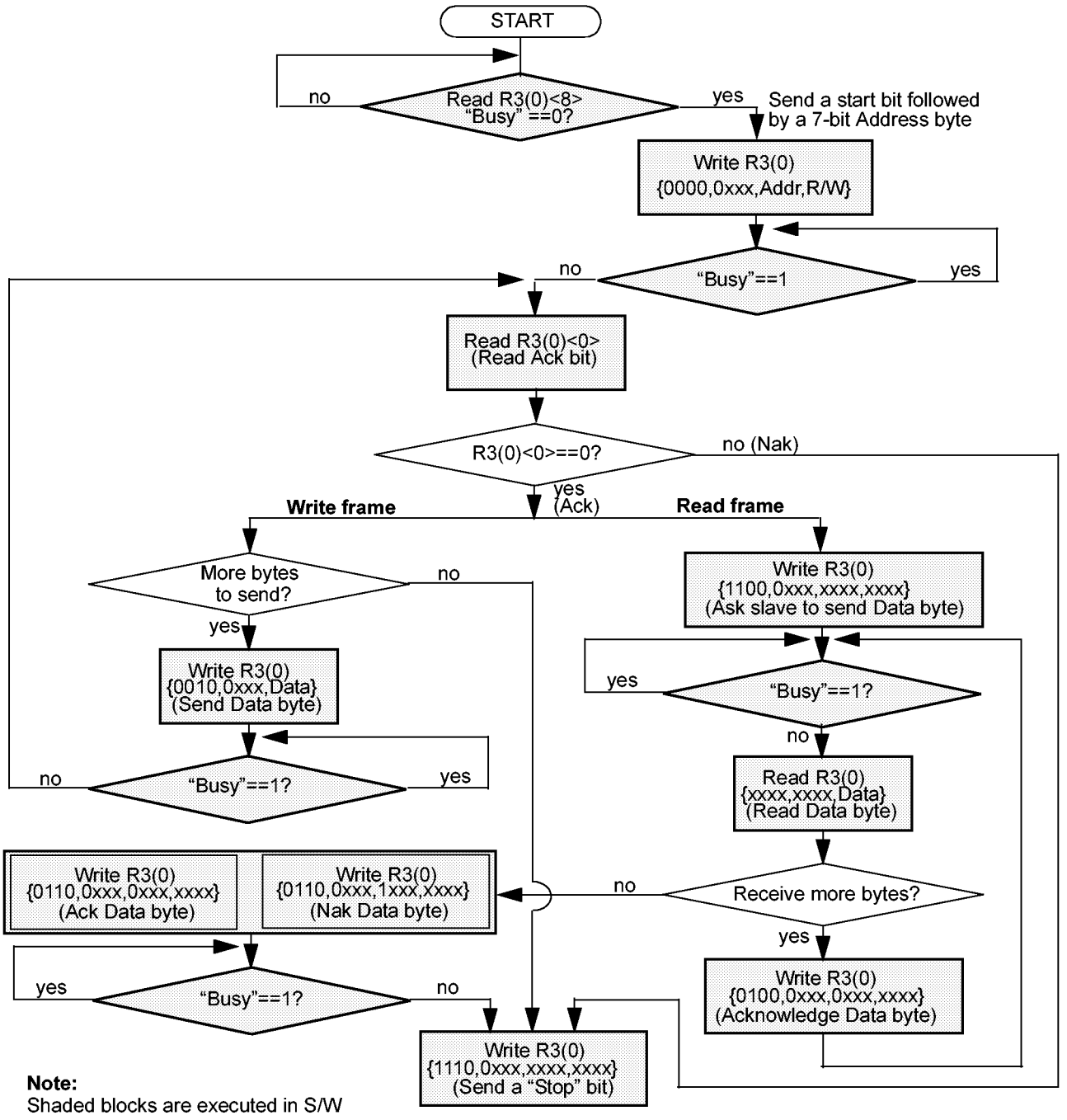


Figure 15. Master Mode

MEMORY ALLOCATION FOR CURSOR'S BITMAP (Continued)

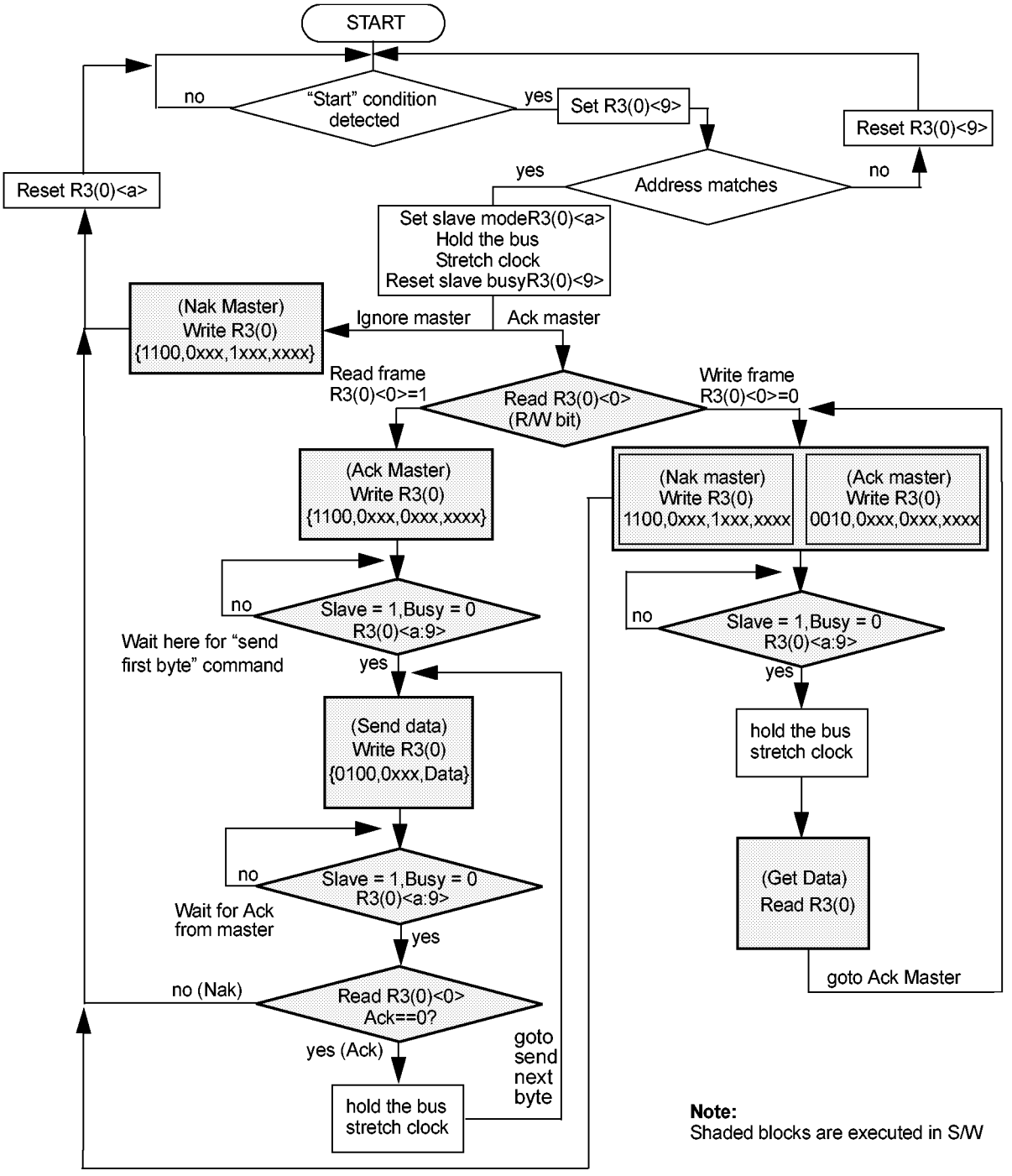


Figure 16. Slave Mode

Note: If a "Stop" condition is detected at any point, the hardware resets the "Slave" bit (R3(0)<a>, and releases the I^2C bus.

REGISTER SUMMARY

Table 14. Register Utilization

BANK	BANK Sub Address	READ Register	WRITE Register	Description
Bank0	7	dir1		16-bit I/O port 1 direction control
	6	dir0		16-bit I/O port 0 direction control
	5	port1		9-bit I/O port 1
	4	port0		16-bit I/O port 0
	3	I2C_int		I^2C interface register
	2	pll_freq		PLL frequency control
	1	write control register		Cursor palette gauge Write control register
	0	pwm_data9		14-bit PWM9 data
Bank1	7	wdt_smr_ctl		SMR and WDT control
	6	clock_ctl		Clock control (switch VCO/DOT)
	5	cap_1s_ctl		Counter timers control
	4	ADC_ctl		A/D converter control
	3	standard_ctl		Output H/VSYNC/blnk control
	2	9-bit counter	STOP/WDT	Stop and WDT instructions, 9-bit counter
	1	sclk_freq		Stop/sleep/normal mode
	0	clamp_pos		Defines position of video clamp pulse
Bank2	7	CGROM offset register		CGROM offset register
	6	Reserved		Reserved
	5	pwm_data6		8-bit PWM 6 data
	4	pwm_data5		8-bit PWM 5 data
	3	pwm_data4		8-bit PWM 4 data
	2	pwm_data3		8-bit PWM 3 data
	1	pwm_data2		8-bit PWM 2 data
	0	pwm_data1		8-bit PWM 1 data
Bank3	7	output palette		Output palette
	6	palette_color		Display palette color/underline color
	5	capture_data	I^2C slave addr.	Capture register data
	4	osd_control		On screen display control
	3	attribute_data	vram_data	Character attribute/video RAM data
	2	ch_x1_lo_x3	cg_attribute	Character multiple/character graphics attribute
	1	lo_x2_mid_x3	cg_nxt_prv	Character multiple/next or previous data
	0	hi_x2_hi_x3	cg_current	Character multiple/current data

REGISTER DESCRIPTION

The register file of the Z9037X is organized into four banks, selectable by writing to bits 5 and 6 ("bank switch" bits) in the Status Register of the Z89C00 core. All registers are mapped into an external register space of the Z89C00 DSP core and each bank consists of 8 registers. The Status register is available for reading or writing at any time. In order to access the register file, the appropriate bank of registers should be selected. The software effectively keeps track of which register bank is accessible at any time.

Table 15. Bank Assignments

Bank	Status Register	Bank Functionality
Bank0	xxxx xxxx x00x xxxx b	I/O ports, I²C interface, PLL frequency
Bank1	xxxx xxxx x01x xxxx b	Control registers
Bank2	xxxx xxxx x10x xxxx b	PWM1–PWM6—8 bit CGROM Offset Register
Bank3	xxxx xxxx x11x xxxx b	OSD, palette control

Bank0 (I/O Ports, I²C Interface, PLL Frequency, PWM9)

The Port/PWM bit defines the mode of the PWM9 output. When set to a "1", the PWM9 output monitors the data specified by the Port_data field. Otherwise, the PWM_data field defines the waveform on the PWM9 pin.

Table 16. Register2—R2(0) PLL Frequency Data Register

Reg Field	Bit Position	R	W	Data	Description
M_disable	f---------------	R	W	1 0	I²C Master interface disabled I²C Master interface enabled–POR
S_disable	-e--------------	R	W	1 0	I²C Slave interface disabled I²C Slave interface enabled–POR
Reserved	--dcba98--------	R W			Return "0" No effect
I²CM_mux	--d------------	R	W	1 0	Select I²MSD2, I²MSC2–POR Select I²MSD1, I²MSC1
I²C_Out_ Resistance	---c----------	R	W	1 0	600Ω output resistance Normal CMOS port output resistance–POR
I²C_speed_ range	----b----------	R	W	1 0	Low speed range (10 kHz, 50 kHz) High speed range (100 kHz, 400 kHz)–POR
Reserved	-----a----------	R W			Return "0" No effect
P46/HSYNC	------9---------	R	W	1 0	HSYNC logic takes input from Pin 46 HSYNC logic takes input from HSYNC pin–POR
P07/ComSYNC	-------8--------	R	W	1 0	Composite Sync Output P07 I/O–POR
PLL_data	--------76543210	R	W	xx	PLL divider = 256 + xx

If the master or slave I^2C interface is enabled, the correspondent I/Os (Port01 and Port02 for the slave, Port11 and Port12 for the master) must be assigned as outputs.

The VCO, DOT, and SCLK frequency are defined as:

$$F_{VCO} = F_{DOT} = F_{SCLK} = XTAL * (256 + PLL_{DATA})$$

Therefore,

XTAL = 3.2768 kHz

Upon PO,R the PLL frequency data register is preset to %70, which corresponds to the VCO frequency of 12.058 MHz.

The PLL_data field can be loaded with any value from %00. This value corresponds to an SCLK = 256*XTAL up to %FF, which corresponds to an SCLK = 511*XTAL. Because the SCLK frequency is proportional to the frequency of the XTAL, it is impossible to specify the maximum value that can be written into the PLL_data field. It is the customer's responsibility not to exceed the SCLK frequency of 12.5 MHz. For common applications incorporating a 32768-Hz XTAL oscillator, the maximum setting of the PLL_data field in R2(0) is %7D, which corresponds to:

SCLK = 381*XTAL = 12.485 MHz.

Table 17. Register3—R3(0) I^2C Interface Register

Reg Field	Bit Position	R	W	Data	Description
Command	fed----------	R			Return "0"
			W	%D	See full description Table 12.
Toggle	---c----------	R		1	Slave interface
				0	Master interface–POR condition
			W	1	Toggle active I^2C interface
				0	No effect
Reset	----b----------	R			Return "0"
			W	1	Reset Slave I^2C interface if bit <c> = 1
				0	Reset Master I^2C interface if bit <c> = 0
					No effect
Slave_mode	-----a----------	R		1	Slave mode is active
				0	Slave mode is inactive
			W		No effect
SlaveBusy	------9---------	R		1	Slave I^2C interface is busy
				0	Slave I^2C interface is idle
			W		No effect
MasterBusy	-------8--------	R		1	Master I^2C interface is busy
				0	Master I^2C interface is idle
			W		No effect
Data	--------76543210	R		xx	Received data
			W	xx	Data to be sent

Data written to R3(0)<cb> requires 4 cycles before being applied. Consecutive writings to these bits require at least a 6-cycle delay.

The received data is available for reading only when the "busy" bit is reset to a "0". Upon POR, the speed of the I^2C interface is set to "Low".

REGISTER DESCRIPTION (Continued)

Table 18. Register4—R4(0) Port 0 Data Register

Reg Field	Bit Position	R	W	Data	Description
Port_data	fedcba9876543210	R		xxxx	If a port is configured in Input mode, then enter the input data onto the port pins. If a port is configured in Output mode, then the data is written directly to the port data.
			W	xxxx	

Table 19. Register5—R5(0) Port 1 Data Register

Reg Field	Bit Position	R	W	Data	Description
Port_data	-------876543210	R		xxxx	If a port is configured in Input mode, then enter the input data onto the port pins. If a port is configured in Output mode, then the data is written directly to the port data.
			W	xxxx	

Table 20. Register6—R6(0) Port 0 Direction Register

Reg Field	Bit Position	R	W	Data	Description
Port_direction	fedcba9876543210	R	W	xxxx	1: Input mode for corresponding bit 0: Output mode for corresponding bit

Table 21. Register7—R7(0) Port 1 Direction Register

Reg Field	Bit Position	R	W	Data	Description
Port_direction	-------876543210	R		xxxxx	1: Input mode for corresponding bit 0: Output mode for corresponding bit
			W		

Bank1 (Control Registers)

Table 22. Register0—R0(1) Clamp Position Register

Reg Field	Bit Position	R	W	Data	Description
Disable_clamp_1	f---------------	R	W	1 0	ADC0 Clamp generation is disabled ADC0 Clamp generation is enabled
Disable_clamp_2	-e--------------	R	W	1 0	ADC5 Clamp generation is disabled ADC5 Clamp generation is enabled
Reserved	--dc------------	R			Return “0”
			W		No effect
Disable_tip_clamp	--d-------------	R	W	1 0	ADC0 Tip clamp is disabled–POR ADC0 Tip clamp is enabled
Counter_input	---c------------	R	W	1 0	Counter takes input from P06–POR Counter takes input from internal HSYNC Separator
ARenable	----b-----------	R		1	AR enabled
			W	0	AR disabled–POR
Position	---------6543210	R	W	xx	Position of clamp pulse (from leading edge of the H-FLYBACK)

Upon PO,R both disable_clamp bits are set to a "1".

The clamp pulse is generated if it is Enabled (bit <f>) and the SCLK frequency is switched "back" to PVCO. Also, the SVCO/PVCO flag in R6(1) should be reset to "0" before the current HSYNC, regardless whether the SVCO is enabled or disabled.

The clamp position is defined by the "Position" field. The width of the clamp pulse cannot be modified and is set to 1us. The value that can be assigned to the "Position" field should be >%10 and <%7F. The time interval between the leading edge of the H-FLYBACK and the beginning of the clamp pulse can be calculated from:

$$T_{DELAY} = Position \times \frac{1}{TSCLK} = Position \times 82ns$$

Table 23. R1(1) Speed Control Register

Reg Field	Bit Position	R	W	Data	Description
Reserved	f----------				Reserved
	-e----------	R	W	1	Standard interlaced mode (single scan mode)
				0	Double scan mode–POR
H_SHIFT	--dcba98--------	R	W	%D	Shift right in 4 pixels increment–POR = 0
1xHSYNC	--------7-------	R	W	1	1xHSYNC is connected to Port03
				0	1xHSYNC is 2xHSYNC/2–POR
Skip_HSYNC	---------6------	n/a	W	1	Skip next HSYNC
				0	Do not skip next HSYNC
Frame_start	----------5-----	n/a	W	1	Field start initialization
				0	No effect
OSD_black	-----------4----	R	W	1	Next output line is OSD
				0	Next output line is black
Line_buffer_mode	------------3---	R	W	1	Interlaced (OSD/black)
				0	Progressive (OSD/OSD)–POR
2x_RGB	-------------2--	R	W	1	Double RGB output
				0	Normal RGB output–POR
Fast_enable	--------------1-	R	W	1	PVCO/SVCO enabled
				0	PVCO/SVCO disabled–POR
Fast_slow	---------------0	R	W	1	SCLK is 12.058 MHz
				0	SCLK is 32.768 KHz–POR

When a POR, SMR, or WDT reset occurs, both the Fast_enable and Fast/Slow are reset to "0". This event corresponds to an SCLK frequency of 3.2768 kHz.

In order to switch from a 3.2768-kHz SCLK to 12 MHz, the following procedure is *required*:

- Set the H_Position field R6(1)<3:0> to a nonzero value
- Enable the primary and secondary VCOs (set the Fast_enable bit R1(1)<1> to "1")
- Wait for one second (1s) for the 12-MHz PLL to stabilize (approximately 50000 clock cycles). That delay depends on the external PLL filter and may vary significantly
- Switch the SCLK to a fast clock (set Fast/Slow bit R1(1)<0> to "1")
- Simultaneously set the H_Position field R6(1)<3:0> to 0FH and the No_Switch field R6(1)<4> to 1 (no clock switch)

In order to switch from the 12-MHz SCLK to 3.2768 kHz, the following procedure is *required*:

- Switch the SCLK to a 32768-Hz clock (set Fast/Slow bit R1(1)<0> to "0")
- Wait for more than R2(0)<7:0> + 256 clock cycles (approximately 32 µS) for the SCLK to be switched
- Set the HSYNC_DELAY field R6(1)<3:0> to "0FH"
- Disable the primary and secondary VCOs (set the Fast_enable bit R1(1)<1> to "0")

Table 24. Register 2—R2(1) WDT/STOP Mode Control Register

Reg Field	Bit Position	R	W	Data	Description
Counter_value	fedcba987-------	R			Counter on Port06 value
			W		No effect
Reserved	---------65432--	R			Return "0"
			W		No effect
WDT_instr	--------------1-	R		1	Return "0"
			W	0	WDT enable, WDT reset
					No effect
STOP_instr	---------------0	R		1	Return "0"
			W	0	STOP instruction
					No effect

When a POR, SMR or a WDT reset occurs, the WDT is disabled. The WDT can be reenabled only after the PVCO and SVCO are enabled, and the part is switched into a Fast mode (SCLK = 12 MHz). Upon switching the part into a SLOW mode (SCLK = 3.2768 kHz), the WDT halts. Upon returning to the Fast mode, an additional reinitialization of the WDT is necessary.

Table 25. Register 3—R3(1) Standard Control Register

Reg Field	Bit Position	R	W	Data	Description
Counter_ reset	f---------------	R		1	Return "0"
			W	0	Reset Counter on Port06
					No effect
Counter_ON/OFF	-e--------------	R	W	1	Counter on Port06 is ON
				0	Counter is OFF–POR condition
Mask_HVSYNC	--d-------------	R	W	1	Disable HVSYNC output
				0	HVSYNC IN/OUT–POR condition
Char_size_16_18/20	---c------------	R	W	1	16x20 character matrix
				0	16x16 or 16x18 character matrix–POR
Bank0_128/Bank0_256	----b-----------	R	W	1	Extended RAM–128 words
				0	Basic Bank–256 words–POR condition
P07/ComSYNC	-----a----------	R	W	1	Composite SYNC output
				0	P07 I/O–POR condition
Bank0_sel	----ba----------	R	W	00	RAM Bank 00–POR
				01	RAM Bank 01
				10	RAM Bank 02
				11	Reserved
RGBC/Port1	------9---------	R	W	1	SCLK, R<1:0>, G<1:0>, B<1:0>
				0	P16,P08,P10,P13,P18,P15,P14
I^2C_HI/LO_speed	-------8--------	R	W	1	HI speed (400 kHz)
				0	LO speed (100 kHz)–POR condition
I^2C_HI/LO_speed	-------8--------	R	W	1	HI speed (400 kHz/50 kHz)
				0	LO speed (100 kHz/10 kHz)–POR
CGROM bank	--------7-------	R	W	1	Bank1 is selected (starts @%1000)
				0	Bank0 is selected (starts @%0000)
SOVL/P0f	---------6------	R	W	1	Semi-transparency output
				0	P0f output
OSD_on/off	----------5-----	R	W	1	OSD is enabled
				0	OSD is disabled–POR

Table 25. Register 3—R3(1) Standard Control Register (Continued)

Reg Field	Bit Position	R	W	Data	Description
RGB_polarity	----------4----	R	W	1	Negative
				0	Positive
Positive/Negative	----------3---	R	W	1	Negative HVSYNC in output mode
				0	Positive HVSYNC in output mode
SYNC/BLANK	----------2--	R	W	1	HVBLANK outputs
				0	HVSYNC outputs
25/30_Hz and HV_polarity	----------10	R	W		Internal mode *only* (TV Standard)
				10	50 Hz/625 lines support
				00	60 Hz/525 lines support–POR
					External mode *only* (HV Polarity)
				11	Positive
				01	Negative

There are two different bits which define the polarity of the HVSYNC signals. Bit <3> defines polarity of the signals when they are configured as outputs (it does not affect the internal HV–SYNC signals). Bit <1> defines the polarity of the external HV–SYNC signals, affecting the synchronization of the device.

Notes: The composite SYNC is active in internal mode only.

When using the internally-generated COMPOSITE SYNC signal, be sure the SCLK is set to 12.09MHz (R2(0)<7:0> = %71). This action helps ensure the best HSYNC frequency approximation.

Table 26. Register4—R4(1) ADC Control Register

Reg Field	Bit Position	R	W	Data	Description
HW_shift	-ed----------	R		00	Direct (unmodified)–POR
			W	01	4-bit shift left
				10	4-bit shift right
				11	Byte swap
Reserved	---cb----------	R			Return "0"
			W		No effect
HSYNC_edge*	---c----------	R	W	1	HSYNC is leading edge active
				0	HSYNC is trailing edge active–POR
ADC_ref	----b----------	R	W	1	ADCs use AV_{CC} and AGND as reference voltage
				0	ADCs use 2.0V and 1.5V as reference voltage–POR
ADC_select	-----a----------	R	W	1	ADC4, ADC5 select
				0	ADC0, ADC1, ADC2, ADC3 select–POR condition
Reserved	------98--------	R			Return "0"
			W		No effect
ADCspeed	--------76------	R	W	00	Single conversion–POR condition
				01	SCLK/4
				10	SCLK/6
				11	SCLK/8
ADCsource	----------54----	R	W	00	ADC0 (CVI)/ADC4 (P04)–POR
				01	ADC1 (P17)/ADC5
				10	ADC2 (P00)
				11	ADC3 (P05)
ADCdata	------------3210	R		%D	ADC data
			W		No effect

Note: *If HSYNC is Leading Edge Active (R4(1)<c> = 1),the actual interrupt is delayed from the leading edge of HSYNC by 72 cycles (~6uS @12MHz).

ADC0 features a signal range from 1.5 to 2.0 V. This field is always connected to the Composite Video Input pin of a device and can be clamped to a Ref– voltage (1.5V).

ADC1, ADC2, ADC3, and ADC4 have a signal range from 0 to 5.0V. ADC1, ADC2, and ADC3 are multiplexed with P17, P00, and P05 ports. In order to use the pin as an ADC input, the corresponding port should be set up as an input (refer to R4(0) and R6(0)).

ADC5 features a signal range from 1.5 to 2.0 V. For this field, the input signal can be clamped to a Ref+ voltage (2.0V).

Table 27. Register5—Timer Control Register

Reg Field	Bit Position	R	W	Data	Description
CAPint_r	f---------------	R		1	Rising edge is captured
				0	No rising edge is captured
			W	1	Reset flag
				0	No effect
CAPint_f	-e--------------	R		1	Falling edge is captured
				0	No falling edge is captured
			W	1	Reset flag
				0	No effect
Tout_1s	--d-------------	R		1	Timeout of 1s timer
				0	No timeout of 1s timer
			W	1	Reset flag
				0	No effect
Tout_CAP	---c------------	R		1	Timeout of Capture timer
				0	No timeout of Capture timer
			W	1	Reset flag
				0	No effect
Reserved	----ba----------	R			Return “0”
			W		No effect
Speed_1s	------98--------	R	W	00	1s
				01	250 ms
				10	62.5 ms
				11	15.625 ms
Port09/ CAP_int*	--------7-------	R	W	1	int2 source is Port09
				0	int2 source is Capture timer
CAP_halt*	---------6------	R	W	1	Capture timer is halted
				0	Capture timer is running
CAP_edge*	----------54----	R	W	00	No Capture
				01	Capture on rising edge only
				10	Capture on falling edge only
				11	Capture on both edges
CAP_glitch*	------------32--	R	W	00	Glitch filter is disabled
				01	<8TSCLK is filtered out
				10	<32TSCLK is filtered out
				11	<128TSCLK is filtered out
CAP_speed*	--------------10	R	W	00	SCLK/4
				01	SCLK/8
				10	SCLK/16
				11	SCLK/32

Note: *Resetting of any Capture Timer flags does not modify Capture Counter and/or Capture register data. When the glitch filter is enabled, the duration of the pulse is decreased by CAP_glitch value.

REGISTER DESCRIPTION (Continued)

Table 28. Register6—Clock Switch Control Register

Reg Field	Bit Position	R W	Data	Description
Reserved	fedcba9876------	R		Return "0"
		W		No effect
SVCO/PVCO	----------5-----	R	1	SCLK = SVCO (flag)
			0	SCLK = PVCO (flag)
		W	1	Switch SCLK to PVCO
			0	No effect
No_Switch	----------4----	R W	1	SCLK = PVCO, no clock switching—POR
			0	Clock switching is enabled
H_Position	------------3210	R W	%D	Defines delay of Hint by 4D SCLK cycles

The Clock switch control register defines the source of the SCLK fed into the Z89C00 core. The block diagram of the clock switch circuit is presented in Figure 17.

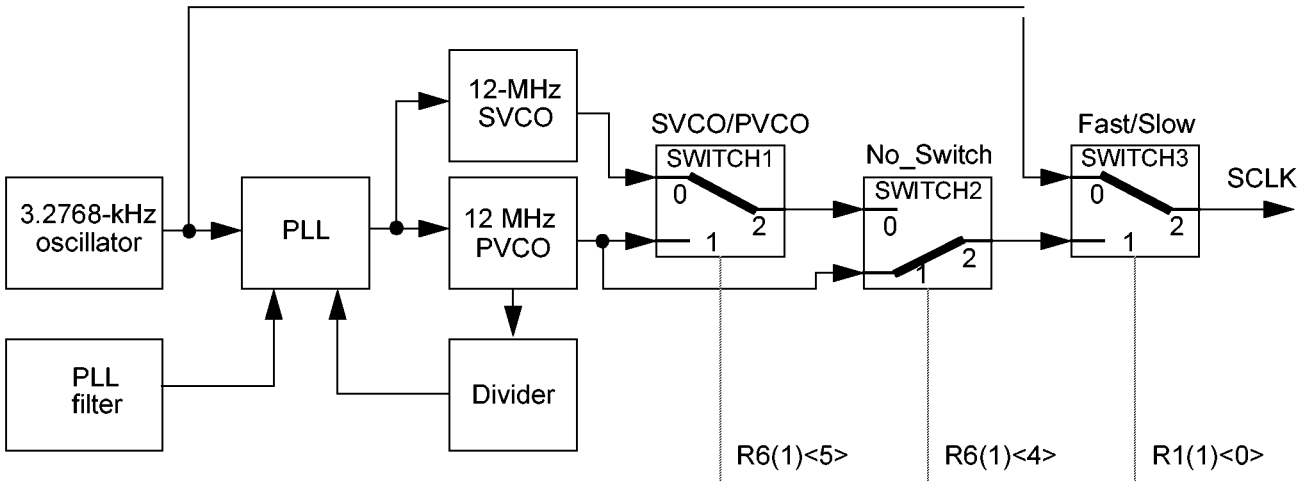


Figure 17. Clock Switching Block Diagram

H_Position

When a fast clock is enabled, the H_Position must be set to 0FH. The actual adjustment of the horizontal position should be performed by R1(1)<c:8>.

No_Switch

The No_Switch bit is set to "1" (no clock switch) upon power-up reset. The No_Switch bit must be set to 1 (no clock switch) if a fast clock is enabled. In such a case, the system clock is permanently set to a primary VCO (PVCO) in the Z9037X and does not require a software clock control switch within a HSYNC_ISR.

Table 29. Register7—R7(1) Interrupts/WDT/SMR Control Register

Reg Field	Bit Position	R	W	Data	Description
Int_priority	fed----------	R	W	x	See Table 30
Int_mask	---cba----------	R	W	1xx	int2 is enabled
				0xx	int2 is disabled
				x1x	int1 is enabled
				x0x	int1 is disabled
				xx1	int0 is enabled
				xx0	int0 is disabled
WDTspeed	------98--------	R	W	00	1.83 ms
				01	7.68 ms
				10	31.12 ms
				11	124.8 ms
SMRflag	--------7-------	R		0	No Stop-Mode Recovery–POR
				1	Stop-Mode Recovery
			W		No effect
SMR polarity	---------6------	R	W	0	OR of all SMR sources
				1	NAND of all SMR sources
SMRsource	----------543210	R	W	xx	Bit which corresponds to a "1" in xx binary representation is active
smr5	----------5-----				p09
smr4	-----------4----				p14
smr3	------------3---				p13
smr2	-------------2--				p12
smr1	--------------1-				p11
smr0	---------------0				p10

The final result of the Stop-Mode Recovery (SMR) is RESET. Ports selected for SMR must be assigned as inputs, while the other SMR ports must be assigned as outputs exhibiting a nonactive value. If any SMR source is active, and the Stop Mode is executed, the part resets immediately.

The priority of the Z89C00 core interrupts is set to int0 > int1 > int2. These priorities can not be changed and are embedded into the core. However, the Z9037X architecture provides the customer with an ability to change the priority the of interrupts by switching the interrupt sources between interrupt inputs of the Z89C00 core. The priority table provides the correspondence between HSYNC, VSYNC and 1s/CAP interrupts sources, and int0, int1 and int2 interrupts inputs of the Z89C00 core (Table 30).

Table 30. Interrupt Priority

Int_Priority Field	HSYNC Is Switched To:	VSYNC Is Switched To:	1s/CAP Is Switched To:
0 0 0	int0	int1	int2
0 0 1	int0	int2	int1
0 1 0	int1	int0	int2
0 1 1	int2	int0	int1
1 0 0	int1	int2	int0
1 0 1	int2	int1	int0

REGISTER DESCRIPTION (Continued)

Bank2 (PWM Registers)

Table 31. Register0–Register5—R0(2)–R5(2) PWM 1–6 Registers

Reg Field	Bit Position	R W	Data	Description
Reserved	fedcba98--------	R W		Return "0" No effect
PWM_data	--------76543210	R W	xx	8-bit PWM data

All of the PWMs feature push-pull. The outputs of all PWMs are staged by one PVCO clock. The repetition frequency of the PWM output signals can be calculated from:

$$F_{PWM} = \frac{F_{PVCO}}{8-256} = \frac{12MHz}{2048} = 6kHz$$

Upon reset, the PWM_data registers are not initialized; however, the PWM output is set to "0". Because the PWM is clocked with PVCO, it is recommended to initialize the PWM_data before enabling PVCO.

Bank3 (On Screen Display [OSD] registers)

Table 32. Register0–Register2—R0(3)–R2(3) Character Multiple Registers, Read Only

Reg Name	CGROM Data	Reg Address	Description
cgrom_x2_hi	ffeeddccbbaa9988	R0(3)	High word of double size character R4(3)<6> = 0
cgrom_x3_hi	fffeeedddcccbbba		High word of triple size character R4(3)<6> = 1
cgrom_x2_lo	7766554433221100	R1(3)	Low word of double size character R4(3)<6> = 0
cgrom_x3_mid	aa99988877766655		Middle word of triple size character R4(3)<6> = 1
cgrom_x1	fedcba9876543210	R2(3)	Single size character R4(3)<6> = 0
cgrom_x3_lo	5444333222111000		Low word of triple size character R4(3)<6> = 1

The detailed description of the Character multiplier registers is provided on page 12.

Table 33. Register0–Register1—R0(3)–R1(3) Shift Registers, Write Only

Reg Name	CGROM Data	Reg Address	Description
current_reg	fedcba9876543210	R0(3)	current line shift register
next/previous_reg	fedcba9876543210	R1(3)	next/previous line shift register

Registers R3(3) and R0(3) must be loaded with the video data one time every 16 cycles. To support smoothing, register R1(3) must be updated every 16 cycles. The current line register should be loaded first, followed by next/previous register during the next cycle. The next/previous register should be loaded only if smoothing/fringing attributes are activated for the current character. If neither of these registers are loaded, the space character is displayed. There is no difference between loading "0000"h into either of the registers or not loading them at all.

Table 34. Register2—R2(3) Attributes Register, Write Only

Reg Field	Bit Position	Data	Description
Reserved	f---------------	x	No effect
Background color	-edc------------	000 001 010 011 100 101 110 111	Black Blue Green Cyan Red Magenta Yellow White
Foreground color NOT PALETTE MODE	----ba9---------	%D	Same as Background mode
Palette selection PALETTE MODE	----ba----------	00 01 10 11	Palette0 Palette1 Palette2 Palette3
2nd_underline PALETTE MODE	------9---------	1 0	Second Underline is active Second Underline is NOT active
1st_underline	-------8--------	1 0	First Underline is active First Underline is NOT active
Shift_video	--------7-------	1 0	Video signal is delayed by 8 pixels Standard character positioning
Semi-Transparent	---------6------	1 0	Transparent background Background color defined by “background color” field
Blinking	----------5-----	1 0	Blinking character Not blinking character
Italic	-----------4----	1 0	Italic character Not italic character
Color_delay	------------32--	00 01 10 11	Character color changes instantly Color changes with 4 pixels delay Color changes with 8 pixels delay Color changes with 12 pixels delay
Left Shadow	--------------1-	1 0	Left Shadow No left shadow
Right Shadow	---------------0	1 0	Right Shadow No right shadow

Note: The shadow is inactive if smoothing is off.

There is no special attribute bit for S_Overlay. The S_Overlay signal is multiplexed with Port0F and goes High when the background is transparent. S_Overlay can be used to generate a semi-transparent OSD if the external hardware supports both the mixing of background signals and OSD.

The attributes register should be loaded 8 cycles after the current line register R0(3) is loaded. Loading of the attributes register enables the OSD logic during the next 16 cycles. If the attributes register is not loaded, there is no active OSD, even if the current line register R0(3) is loaded.

Table 35. Register3—R3(3) Attributes Register, Read Only

Reg Field	Bit Position	Data	Description
		Same as R2(3)	

REGISTER DESCRIPTION (Continued)

The data read from the attribute register is a combination of attribute fields of the most recent displayed character and control character codes loaded into the attribute_data register. The character codes are fetched from Video RAM and should be loaded into the attribute_data register R3(3). Bit <f> of the attribute_data register (upon reading) indicates whether the most recent character was a control or displayed character. The data read from the attribute_data register must be directly loaded into an attribute register R2(3).

Table 36. Register3—R3(3) Attribute Data Register, Write Only

Reg Field	Bit Position	Data	Description
VRAM_data	fedcba9876543210	xxxx	Character code fetched from VRAM

Loading VRAM data into an attribute_data register will initialize a CGROM access cycle. Four clock cycles after the LD instruction, the Z89C00 core is halted for three clock cycles in order to fetch the data from CGROM and latch it into a CGROM data capture register. After the CGROM data is latched, the core operations are resumed. When a control character code is loaded into the attribute_data register, the CGROM data from address "0000"h is fetched. Therefore, it is recommended to place a space character at location "0000"h in CGROM.

Table 37. Register4—R4(3) OSD Control Register

Reg Field	Bit Position	R	W	Data	Description
Underline	fe----------	R	W	1x 0x x1 x0	Second underline is active Second underline is inactive First underline is active First underline is inactive
OSD/CCD	--d----------	R	W	1 0	OSD mode CCD mode
CCD_top/btm	---c----------	R	W	1 0	The upper byte in VRAM is used The lower byte in VRAM is used
Italic_shift	----ba98--------	R	W	x	Defines delay of the character
Blink_off/on	--------7-------	R	W	0 1	Blinking character is displayed Blinking character is NOT displayed (hidden)
MPX_bus	---------65-----	R	W	00 01 10 11	x1 character size x2 character size x3 character size Reserved
CGROM scan_line	----------43210	R	W	%D	Defines CGROM addressing

The Underline field should be set by the firmware during the line/lines of the OSD when the second/first underline is active. The bits are ANDed with the 2nd/1st underline active fields of data loaded into an attribute register R2(3), allowing the screen character to be underlined.

The Italic shift field defines the delay of current video data. Typically, it is used to generate italic characters. The firmware decrements by "1" (the value of the Italic_shift field) for each consecutive line. The video signal is delayed only for those characters for which the R2(3)<4> ("italic") bit is set to a "1".

Table 38. Register5—R5(3) Capture Register, Read Only

Reg Field	Bit Position	R	W	Data	Description
Cap_data	fedcba9876543210	R		%xxxx	16-bit captured data
Reserved	fedcba98-------0	R			Return "0"
			W		No effect
I2C_saddr	--------7654321-		W	%DD	I^2C Slave interface address

Table 39. Register6—R6(3) Palette Control Register

Reg Field	Bit Position	R	W	Data	Description
Palette	f---------------	R	W	1	Palette mode is active
				0	Palette mode is INACTIVE
Underline color	-edc----------	R	W	000	Black
				001	Blue
				010	Green
				011	Cyan
				100	Red
				101	Magenta
				110	Yellow
				111	White
Palette1	----ba9---------	R	W	%D	Same as Underline color
Palette0	-------876------	R	W	%D	Same as Underline color
Palette3	----------543---	R	W	%D	Same as Underline color
Palette2	------------210	R	W	%D	Same as Underline color

Upon POR the palette control register is reset to "0".

Table 40. Register7—R7(3) Output Palette Control Register

Reg Field	Bit Position	R	W	Data	Description
OVERLAY_delay	fedc----------	R	W		OVL and SOVL delay value—%00–POR condition
Background_on/off	----b----------	R	W	1	Master background is on
				0	Master background is off–POR condition
Background_color	-----a98--------	R	W	%D	Defines the color of the Master background (the same as the Palette)
MBG_color	-----a98--------	R	W	%D	Defines the color of the Master background (the same as the Palette)
AttrSelect	--------76------	R	W	00	1st underline—POR
				01	Semi-transparency
				10	Blinking
				11	CGROM bank select
Smoothing	----------5-----	R	W	0	Smoothing logic disabled—POR
				1	Smoothing logic enabled
Cursor Write Enable	----------4----	R			Return "0"
			W	0	Cursor parameters write disabled—POR
				1	Cursor parameters write enabled
Palette #	------------3210	R	W	%D	Palette number

Upon POR, the Output palette register is set to "0"–digital output.

ADDITIONAL CONTROL REGISTERS (AR)

Additional Control Registers (AR) are implemented to control new peripheral blocks like palette banks and memory management. To activate ARs, R0(1)<b> should be set to "1". ARs can be disabled by setting R0(1)<b> = 0, (POR) for software backward compatibility, or if access to the RAM location %1FF is required.

128 eight-bit control registers (referred as AR or ARx<y:z>) are implemented utilizing RAM mapped I/O access. Location %1FF in the RAM is used to address up to 128 byte-width ARs. The AR number and written data are encoded into the data field as illustrated in Figure 18:

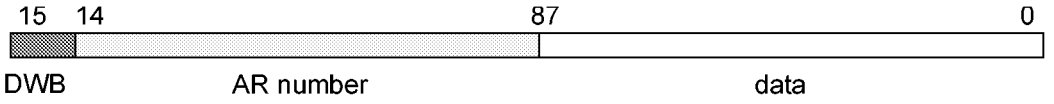


Figure 18. AR Register Format

Upon writing to the address %1FF, the Data Write Bit (DWB) and AR number are latched (depending on whether the DWB data field is either written to the selected port or discarded). The AR number and correspondent data are read after reading from the previously-latched DWB address %1FF.

In order to write to the AR, the next data should be written to the address %1FF; DWB should be set to "1", the port number should be specified in bits 8–14, and actual data should be specified in bits 0–7.

Example:
```
LD   A, #(%8000 + 29*256 + %57); write 57 (hex) into the AR29
LD   %1FF, A              ;
```

Note: The DWB and port number is latched for possible further reading.

In order to read from the AR, the address should be previously latched by writing it to the address %1FF with DWB set to "0". Bits 0–7 have no meaning. The bits are not going to be written in this mode, so only the port number is latched.

Example:
```
LD   A, #%1E00            ; latch AR30, data is not written
LD   %1FF, A              ;
LD   A, %1FF              ; read from AR30-%1EXX, where XX is current content
```

At least one cycle delay (NOP) is required between two consecutive accesses to the AR. If access is performed by two-cycle instruction, no delay is necessary.

External memory should exhibit access times less than 60 ns.

Color Palette Assignment

The Z9037X features a total of 16 color palettes. The first 8 of them are fixed, while the remaining 8 are programmable. Palette selection is performed by setting R7(3)<3:0>. Fixed palettes are indicated in Table 41.

Table 41. Fixed Palate Color Assignment (Color0 is Black; Color7 is White)

		Color1			Color2			Color3			Color4			Color5			Color6		
Palette #	**Description**	**R**	**G**	**B**	**R**	**G**	**B**	**R**	**G**	**B**	**R**	**G**	**B**	**R**	**G**	**B**	**R**	**G**	**B**
0	Digital RGB	00	00	11	00	11	00	00	11	11	11	00	00	11	00	11	11	11	00
1	Analog RGB	00	00	11	00	11	00	00	11	11	11	00	00	11	00	11	11	11	00
2	Greyscale_1	01	01	01	10	10	10	11	11	11	00	00	00	01	01	01	10	10	10
3	Greyscale_2	00	00	00	01	01	01	01	01	01	10	10	10	10	10	10	11	11	11
4	RGB_Cyan_2Grey	00	00	11	00	11	00	00	11	11	11	00	00	01	01	01	10	10	10
5	RGB_Magenta_2Grey	00	00	11	00	11	00	01	01	01	11	00	00	11	00	11	10	10	10
6	RGB_Yellow_2Grey	00	00	11	00	11	00	01	01	01	11	00	00	10	10	10	11	11	00
7	StarSight	00	11	11	10	11	10	10	10	10	11	01	01	11	11	10	11	11	00

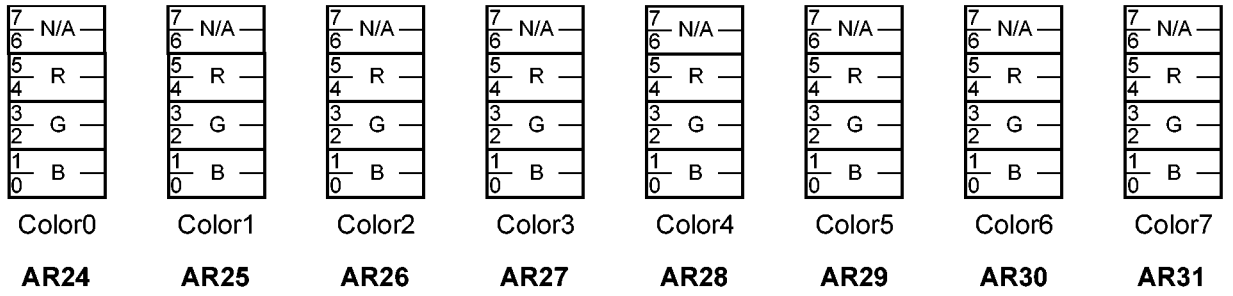


Figure 19. Programmable Palette Control at AR Register

Programmable palettes (# 8–15) are mapped to AR0–AR63 (8 registers per palette). The register and bit assignments for Palette # 11 are indicated Figure 19.

Programmable palettes are grouped into 2 banks (palettes 8–11 and 12–15). Palettes in the bank cannot be modified if another palette from the same bank is displayed. If on-the-fly palette modifications are required, an interleaving palette bank access should be implemented. In this implementation, one palette bank is used to display 4 colors, while the other bank is intended for updating.

Table 42. Additional Control Registers

AR #	Name	Bit position	Data	Function
0	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color0—R1R0G1G0B1B0
1	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color1—R1R0G1G0B1B0
2	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color2—R1R0G1G0B1B0
3	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color3—R1R0G1G0B1B0
4	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color4—R1R0G1G0B1B0
5	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color5—R1R0G1G0B1B0
6	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color6—R1R0G1G0B1B0
7	Palette_8	76------	%D	Reserved
		--543210	%DD	Palette8/Color7—R1R0G1G0B1B0
8–15	Palette_9	76543210	%DD	Same as AR 0–7 for Palette9
16–23	Palette_10	76543210	%DD	Same as AR 0–7 for Palette10
24–31	Palette_11	76543210	%DD	Same as AR 0–7 for Palette11
32–39	Palette_12	76543210	%DD	Same as AR 0–7 for Palette12
40–47	Palette_13	76543210	%DD	Same as AR 0–7 for Palette13
48–55	Palette_14	76543210	%DD	Same as AR 0–7 for Palette14
56–63	Palette_15	76543210	%DD	Same as AR 0–7 for Palette15
64–123				Reserved
124	PgLocation0	7-------	0	Page0 is located internally–POR
			1	Page0 is located externally
		-6------	0	Internal ROM is enabled–POR
			1	Internal ROM is disabled (low power consumption)
		--543210	%DD	Page0—external (physical) page number
125	PgLocation1	7-------	0	Page1 is located internally–POR
			1	Page1 is located externally
		-6------	0	Reserved
		--543210	1	Page1—external (physical) page number
			%DD	
126	PgLocation2	76543210	%DD	Same as above for Page2
127	PgLocation3	76543210	%DD	Same as above for Page3

VIDEO RAM SPECIFICATION (SUPPORTED DATA FORMATS)

The H/W of the Z9037X supports two different data formats in the VRAM. The first one supports a standard OSD with full set of features (OSD mode–R4(3)<d> = 1). The second format supports reduced features which comply with the recommendations of the FCC on Closed Caption support (CCD mode, R4(3)<d> = 0). In CCD mode, the background color of the characters can not be changed, and the characters are always preset to "black".

In OSD mode, each character occupies a 16-bit word in VRAM. There are two possible character formats defined: a "display" character and a "control" character. The code stored in a "display" character format defines a character code and up to 7 attributes of the character. The "control" character defines up to eight attributes of the next character and is presented on-screen as a space character. The combination of "display" and "control" characters allows the generation of a versatile OSD.

Table 43. Display Character Format—Attribute Data Register R3(3)/Write (OSD Mode)

Reg Field	Bit Position	Data	Description
Control bit	f---------------	0	Display character
Background color*	-edc------------	000	Black
		001	Blue
		010	Green
		011	Cyan
		100	Red
		101	Magenta
		110	Yellow
		111	White
Foreground color* (Not palette mode)	----ba9---------	%D	Same as Background_color
Foreground palette (Palette mode)		00x	Palette 0 (defined in R6(3)<8–6>
		01x	Palette 1 (defined in R6(3)<b–9>
		10x	Palette 2 (defined in R6(3)<5–3>
		11x	Palette 3 (defined in R6(3)<2–0>
Second underline (Palette mode)		xx1	Second underline attribute is active
		xx0	Second underline attribute is inactive
Attribute8	-------8--------	1	Selected attribute (R7(3),76>) is active
		0	Selected attribute (R7(3),76>) is inactive
Character code	--------76543210	%DD	Defines the character in CGROM

Note: *If both the background and foreground colors of a character are set to be the same, the character's background is displayed as transparent.

VIDEO RAM SPECIFICATION (SUPPORTED DATA FORMATS) (Continued)

Table 44. Control Character Format—Attribute Data Register R3(3)/Write (OSD Mode)

Reg Field	Bit Position	Data	Description
Control bit	f---------------	1	Control character
Reserved	-edcba98--------	x	Reserved—do not effect OSD
Shift_video	--------7-------	1 0	Video signal is delayed by 8 pixels Standard character positioning
Semi-Transparent	---------6------	1 0	Semi-Transparent background Background color defined by "background color" field
Blinking	----------5-----	1 0	Blinking character Not blinking character
Italic	-----------4----	1 0	Italic character Not italic character
Color_delay	------------32--	00 01 10 11	Character color changes instantly Color changes with 4 pixels delay Color changes with 8 pixels delay Color changes with 12 pixels delay
Right Shadow	--------------1-	1 0	Right Shadow logic is enabled Right Shadow logic is disabled
Left Shadow	---------------0	1 0	Left Shadow logic is enabled Left Shadow logic is disabled

Smoothing is supported for double-size (x2) and triple-size (x3) characters only.

Upon reset, the background color in OSD mode is "black". The foreground color, background color, blinking, and italic attributes are delayed by a ¾ character. The smoothing attribute is enabled.

In CCD mode, each character occupies 8 bits (one byte) in VRAM. The CCD characters should be mapped into a 16-bit VRAM data field. The H/W supports the compressed placement of the characters in VRAM. Each word in VRAM is represented by a High byte and a Low byte. The currently active byte is selected by R4(3)<c>. The format and data representation in both bytes is exactly the same.

There are two possible character formats defined: a "display" character and a "control" character. The code stored in a "display" character format defines a character code. The "control" character defines up to seven attributes of the next character and is presented on screen as a space character. The combination of "display" and "control" characters allows the generation of a CCD OSD according to the FCC specification.

Table 45. Display Character Format—Attribute Data Register R3(3)/Write (CCD Mode)

Reg Field	Bit Position	Data	Description
Control bit	7-------	0	Display character
Character code	-6543210	%DD	Defines the character in CGROM.

Table 46. Control Character Format—Attribute Data Register R3(3)/Write (CCD Mode)

Reg Field	Bit Position	Data	Description
Control bit	7-------	1	Control character
Transparent	-6------	1 0	Transparent background Background color defined by “background color” field
Blinking	--5-----	1 0	Blinking character Not blinking character
Italic	---4----	1 0	Italic character Not italic character
Foreground color	----321-	000 001 010 011 100 101 110 111	Black Blue Green Cyan Red Magenta Yellow White
First underline	-------0	1 0	Underline attribute is active Underline attribute is inactive

DC AND AC CHARACTERISTICS

Table 47. Absolute Maximum and Minimum Ratings

Sym	Parameter	Min	Max	Units	Conditions
V_{CC}	Power supply voltage	0	7	V	
V_{ID}	Input voltage	–0.3	V_{CC}+0.3	V	Digital inputs
V_{IA}	Input voltage	–0.3	V_{CC}+0.3	V	Analog inputs (A/D0–A/D4)
V_O	Output voltage	–0.3	V_{CC}+0.3	V	All push-pull digital outputs
V_O	Output voltage	–0.3	V_{CC}+0.3	V	PWM outputs (PWM1–PWM8)
I_{OH}	Output current high		–10	mA	one pin
I_{OH}	Output current high		–100	mA	all pins
I_{OL}	Output current low		20	mA	one pin
I_{OL}	Output current low		200	mA	all pins
T_A	Operating temperature	0	70	°C	
T_S	Storage temperature	–65	150	°C	

Table 48. DC Characteristics
(T_A = 0°C to 70°C; V_{CC} = 4.75V to 5.25V; F_{OSC} = 32,768 Hz)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{CC}	Power supply voltage	4.75	5.00	5.25	V	
V_{IL}	Input voltage low	0	0.4	0.2 V_{CC}	V	
V_{IH}	Input voltage high	0.7V_{CC}	3.6	V_{CC}	V	
V_{IHR}	Input voltage High on Reset pin	0.75 V_{CC}	4.2	V_{CC}	V	
V_{PU}	Maximum pull-up voltage			V_{CC}	V	For PWM0–PMW8 only
V_{OL}	Output voltage low		0.16	0.4	V	@ I_{OL} = 1 mA
V_{OH}	Output voltage high	V_{CC}–0.4	4.75		V	@ I_{OH} = –0.75 mA
I_{OL}	Output current low	7.2	12		mA	@ V_{OL} = 0.4v
I_{OL1}	Output current low	12	20		mA	@ V_{OL} = 0.8v
I_{OH}	Output current high	4.0	7.0		mA	@ V_{OH} = V_{CC}–0.4
I_{OH1}	Output current high	16	20		mA	@ V_{OH} = 2.4v
I_{OL}	Output current Low	0.35	0.65		mA	@ V_{OL} = 0.4v
I_{OL1}	Output current Low	0.65	1.1		mA	@ V_{OL} = 0.8v
I_{OH}	Output current High	0.35	0.65		mA	@ V_{OH} = V_{CC}–0.4
I_{OH1}	Output current High)	1.1	2.5		mA	@ V_{OH} = 2.4V
V_{XL}	Input voltage XTAL1 low			0.3 V_{CC}	V	External clock generator driven
V_{XH}	Input voltage XTAL1 high	0.6 V_{CC}			V	
I_{IR}	Reset input current	40	90	150	µA	V_{RL} = 0V
I_{IL}	Input leakage	–3.0	0.01	3.0	µA	@ 0V and V_{CC}
I_{CC}	Supply current		60	100	mA	All ports are inputs, RGB is in analog mode

Table 48. DC Characteristics (Continued)
(T_A = 0°C to 70°C; V_{CC} = 4.75V to 5.25V; F_{OSC} = 32,768 Hz)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{CC}	Supply current		30	50	mA	All ports are inputs, RGB is in analog mode
I_{CC1}	Supply current		5	10	mA	Sleep mode @ 3.2768 kHz
I_{CC2}	Supply current		50	100	µA	Stop mode all PWM outputs are @ V_{IN} = 0V

Table 49. AC Characteristics*
(T_A = 0°C to 70°C; V_{CC} = 4.75V to 5.25V; F_{OSC} = 32,768 Hz)

Sym	Parameter	Min	Typ	Max	Units
T_{PC}	Input clock period	16	32	100	µS
T_{RC}, T_{FC}	Clock input Rise and Fall		12		ns
TD_{POR}	Power on reset delay	0.8	1.2		S
TW_{RES}	Power on reset minimum width			5 TPC	µS
TD_{HS}	HSYNC incoming signal width	1	10	15	µS
TD_{VS}	VSYNC incoming signal width	1	200	10000	µS
TD_{ES}	Time delay between leading edge of VSYNC and HSYNC in EVEN field	–12	0	+12	µS
TD_{OS}	Time delay between leading edge of VSYNC and HSYNC in ODD field	20	32	44	µS
TW_{HVS}	HSYNC/VSYNC edge width		0.5	2.0	µS

Note: *All timing of the I^2C bus interface are defined by related specifications of the I^2C bus interface.

Table 50. V1, V2, and V3 (R,G,B) Analog Output

	Output Voltage (30kΩ Load)			Settling Time
	@ V_{CC} = 4.75V	@ V_{CC} = 5.00V	@ V_{CC} = 5.25V	70% of DC Level, 10pF Load
data = 00	0.00V–0.65V	0.00V–0.70V	0.00V–0.75V	<50ns
data = 01	1.70V–0.20V	1.80V–0.20V	1.90V–0.20V	
data = 10	2.80V–0–25V	2.90V–0.25V	3.00V–0.25V	
data = 11	3.90V–0.30V	4.00V–0.30V	4.10V–0.30V	

DC AND AC CHARACTERISTICS (Continued)

Table 51. ADC0, ADC5/Small Range*
(1.5–2.0V; T_A = 0°C to 70°C; V_{CC} = 4.75V to 5.25V)

Sym	Parameter	Min	Typ	Max	Units
U_{R-}	Clamping voltage at ADC0	1.0	1.5	2.0	V
U_{R+}	Clamping voltage at ADC5	0.4+U_{R-}	0.5+U_{R-}	0.6+U_{R-}	V
ADC_0	Input voltage for level 0	U_{R-}–(U_{R+}+U_{R-})/15	U_{R-}	U_{R-}+(U_{R+}–U_{R-})/15	V
ADC_1	Input voltage for level 1	U_{R-}	U_{R-}+(U_{R+}–U_{R-})/15	U_{R-}+2(U_{R+}–U_{R-})/15	V
ADC_2	Input voltage for level 2	U_{R-}+(U_{R+}–U_{R-})/15	U_{R-}+2(U_{R+}–U_{R-})/15	U_{R-}+3(U_{R+}–U_{R-})/15	V
ADC_3	Input voltage for level 3	U_{R-}+2(U_{R+}–U_{R-})/15	U_{R-}+3(U_{R+}–U_{R-})/15	U_{R-}+4(U_{R+}–U_{R-})/15	V
ADC_4	Input voltage for level 4	U_{R-}+3(U_{R+}–U_{R-})/15	U_{R-}+4(U_{R+}–U_{R-})/15	U_{R-}+5(U_{R+}–U_{R-})/15	V
ADC_5	Input voltage for level 5	U_{R-}+4(U_{R+}–U_{R-})/15	U_{R-}+5(U_{R+}–U_{R-})/15	U_{R-}+6(U_{R+}–U_{R-})/15	V
ADC_6	Input voltage for level 6	U_{R-}+5(U_{R+}–U_{R-})/15	U_{R-}+6(U_{R+}–U_{R-})/15	U_{R-}+7(U_{R+}–U_{R-})/15	V
ADC_7	Input voltage for level 7	U_{R-}+6(U_{R+}–U_{R-})/15	U_{R-}+7(U_{R+}–U_{R-})/15	U_{R-}+8(U_{R+}–U_{R-})/15	V
ADC_8	Input voltage for level 8	U_{R-}+7(U_{R+}–U_{R-})/15	U_{R-}+8(U_{R+}–U_{R-})/15	U_{R-}+9(U_{R+}–U_{R-})/15	V
ADC_9	Input voltage for level 9	U_{R-}+8(U_{R+}–U_{R-})/15	U_{R-}+9(U_{R+}–U_{R-})/15	U_{R-}+10(U_{R+}–U_{R-})/15	V
ADC_A	Input voltage for level A	U_{R-}+9(U_{R+}–U_{R-})/15	U_{R-}+10(U_{R+}–U_{R-})/15	U_{R-}+11(U_{R+}–U_{R-})/15	V
ADC_B	Input voltage for level B	U_{R-}+10(U_{R+}–U_{R-})/15	U_{R-}+11(U_{R+}–U_{R-})/15	U_{R-}+12(U_{R+}–U_{R-})/15	V
ADC_C	Input voltage for level C	U_{R-}+11(U_{R+}–U_{R-})/15	U_{R-}+12(U_{R+}–U_{R-})/15	U_{R-}+13(U_{R+}–U_{R-})/15	V
ADC_D	Input voltage for level D	U_{R-}+12(U_{R+}–U_{R-})/15	U_{R-}+13(U_{R+}–U_{R-})/15	U_{R-}+14(U_{R+}–U_{R-})/15	V
ADC_E	Input voltage for level E	U_{R-}+13(U_{R+}–U_{R-})/15	U_{R-}+14(U_{R+}–U_{R-})/15	U_{R-}+15(U_{R+}–U_{R-})/15	V
ADC_F	Input voltage for level F	U_{R-}+14(U_{R+}–U_{R-})/15	U_{R+}	U_{R-}+16(U_{R+}–U_{R-})/15	V
R_{IN}	Input impedance	1			MΩ

Note: *The Input voltage level indicated in the table is a switch point from one ADC level to another. In order to be in the middle of the level half, LSB ((U_{R+}–U_{R-})/(15*2)) should be added. The Input voltage should be prorated accordingly if V_{CC} is changed

ANALOG RGB

The RGB outputs in analog mode are implemented as controlled current sources with an internal load. These outputs display gamma-corrected, V_{CC}-prorated characteristics.

Table 52. RGB Voltage Specifications*

Parameter	Min	Typical	Max	Units
Supply voltage	4.5	5.0	5.5	V
Full scale voltage	1.8V	2.00V (0.40 * V_{CC})	2.2V	V
2/3 scale voltage	1.5V	1.65V (0.33 * V_{CC})	1.815V	V
1/3 scale voltage	1.125V	1.25V (0.25 * V_{CC})	1.375V	V
Zero scale voltage	—	0.00V (0.00 * V_{CC})	+0.1 V	V

Note: *Measured with 3.9 kΩ load.

Table 53. RGB Time Specifications*

Parameter	Min	Typical	Max	Units
Output rise time		50	65	ns
Output fall time		50	65	ns

Note: *Measured with 3.9 kΩ resistor in parallel with 30 pF capacitor load.

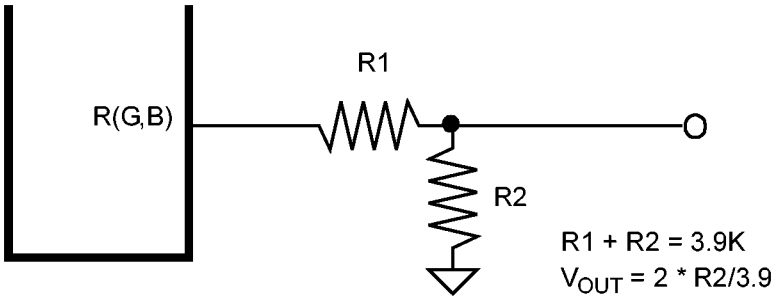


Figure 20. Recommended Application Schematic

HIGH-SPEED OTP PROGRAMMING GENERAL DESCRIPTION

The Z90371 EPROM features 1M bits that are arranged as 64k by 16.

The Z90371 OTP supports programming of one or two words with one programming pulse that is ultimately 4 times faster than the Z89331 programming. High-speed double-word programming is performed by latching two words of data and writing them with one programming pulse. In this mode, the first word should always have ADDR15=1 and the second word should exhibit ADDR15=0. In low-speed single-word programming mode, the address must be incremented sequentially. It is possible to mix both programming modes during one programming operation.

To enter programming mode:

1. Power the chip up ($V_{CC} = V_V$).
2. Bring WE, OE, PCHG to "1".
3. Bring the RESET(V_{PP}) to V_{PP} and XTAL1 (TESTMODE) to 10.5 ±0.25V.
4. Apply 32 negative pulses to the PCHG pin.
5. Start programming.

Table 54. Pin-Out

User Mode	EPROM Mode	User Mode	EPROM Mode	User Mode	EPROM Mode	User Mode	EPROM Mode	User Mode	EPROM Mode
PWM6	Data0	PWM3	Data8	Port08	Addr0	Port16	Addr8	Port0F	Mode0
Port18	Data1	PWM2	Data9	Port09	Addr1	HSYNC	Addr9	Port0E	Mode1
Port02	Data2	Port0A	Data10	Port10	Addr2	VSYNC	Addr10	I2CMSD1	Mode2
Port03	Data3	Port0B	Data11	Port11	Addr3	V1	Addr11	I2CMSC1	Mode3
Port04	Data4	Port0C	Data12	Port12	Addr4	V2	Addr12	Xtal2	PCHG
Port05	Data5	Port0D	Data13	Port13	Addr5	V3	Addr13	PWM1	WR
Port06	Data6	ADC0	Data14	Port14	Addr6	OVL	Addr14	Port17	OE
Port07	Data7	ADC5	Data15	Port15	Addr7	PWM4	Addr15	PWM5	PGM
Xtal1	TstMode	Reset	V_{PP}	IR	GND	ADC2	TstROM		

DETAILED PIN DESCRIPTIONS FOR EPROM MODE

The following is the description of the pinouts and functions for the pins when the device is placed in one of the EPROM modes. Two of the pins are mapped as a High Voltage Detector (HVD) which is a circuit to detect input voltage higher than V_{DD}. This high voltage is referred as "V_H". The output of the HDV is a logic "1" or "0", respectively, depending on whether the input is above or below V_H. The two pins which exhibit HVD are V_{PP} and TstMode. Each are included in the descriptions in Table 55.

Table 55. EPROM Pin Description

Name	Direction	Description
V_{PP}	Input	This pin supplies the programming voltage and current to program the EPROM. It is also used to place the part in program/verify mode when HDV outputs are High. When not in the EPROM program/verify mode, the input should be either V_{DD} or GND.
TstMode	Input	This pin is used to place the part in program/verify mode when HDV output is High. When not in the EPROM program/verify mode, the input should be either V_{DD} or GND.
$\overline{PGM}$	Input	An Active Low programming pulse that applies V_{PP} to the EPROM during programming.
$\overline{OE}$	Input	Active Low output enable. When Low, the output data pins contain data from the EPROM. When High (V_{DD}), the data outputs are tri-stated.
/WE	Input	Active Low write. Upon trailing (positive), edge data is internally latched and ready to be written into EPROM. In double-word program mode, two $\overline{WE}$ pulses are required in order to latch both data words.
$\overline{PCHG}$	Input	Active Low precharge. A negative pulse is required in order for data being read to become valid.
A15–A0	Input	Address bits. In single-word program mode it must be sequentially increment. In double-word program mode first data word should be always written at upper address (A15 = 1), second—at lower address (A15 = 0).
D15–D0	In/Out	Contain data to the EPROM in program mode and from EPROM in read mode.
Mode3–Mode0	Input	Has to be grounded.
TstROM	Input	Has to be grounded.
IR	Input	Has to be grounded.
Unused	n/a	Pins other than mentioned above are not used in EPROM mode and may be left floating. They have internal autolatches which will force the input to either rail.

EPROM MODE DESCRIPTIONS

User Mode:

The standard internal Z90371 mode is accessed from to the EPROM only through the Z89C00 core processor. The external pins are configured as ports, and no access is available to the EPROM from the outside.

Program/Verify Mode

This mode is entered by raising the V_{PP} pin to V_H, which reconfigures the pins for EPROM mode (allowing access from the outside through external pins). In program mode, the V_{PP} pin supplies voltage and current to the EPROM. The V_{DD} pin is raised to V_V to ensure enough programming margin.

DC CHARACTERISTICS

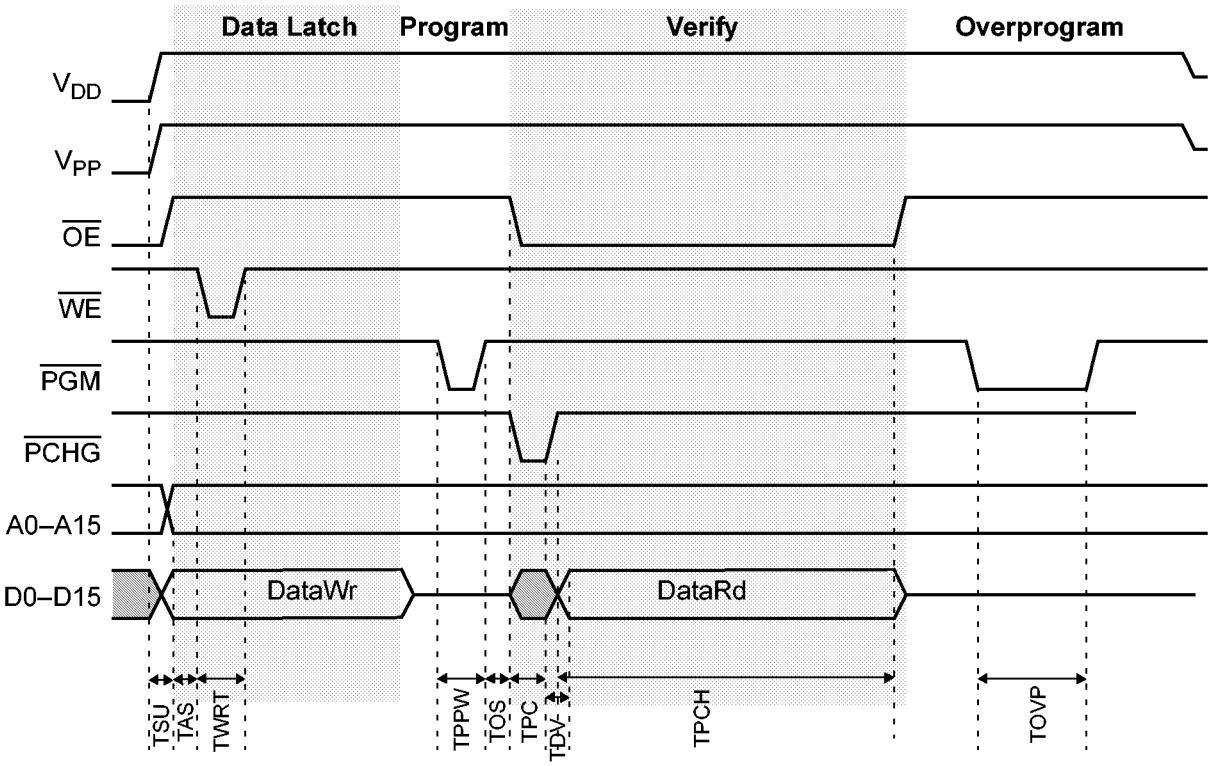
Table 56. DC Characteristics

Read Operating Voltage	V_{DD}	= 4.5V–5.5V
Read Operating Voltage	F_O	= 750kHz–12MHz
Read Operating Voltage	T_O	= 0°C–70°C
Programming Voltage	V_{PP}	= 13.0V ±0.25V
Programming Current (single-word mode)	I_{PP}	= 10mA
Programming Current (double-word mode)	I_{PP}	= 20mA
Prog/verify V_{DD}	V_V	= 6.3V ±0.1V
Programming Temperature	T_{PP}	= 20°C–30°C
Supply Current	I_{CC}	= 120mA max

Notes:
1. During transitions between 5V and 9V, V_{PP} features a transitional leakage path, where V_{PP} shares some of the V_{DD} load.
2. The best-case condition for programming the EPROM is at the upper limit for both V_{PP} and V_V.

Table 57. DC Pin Characteristics

Pin	Parameter	Conditions	Units	Min	Typ	Max
All	V_{HH}, High Voltage Detect active	V_{DD} = 5.0V	Volts	8.5	—	V_{PP}
All	V_{HL}, High Voltage Detect off	V_{DD} = 5.0V	Volts	V_{SS}	—	6.5
All	V_{IH}, Standard	V_{DD} = 5.0V	Volts	3.0	—	V_{DD}
All	V_{IL}, Standard	V_{DD} = 5.0V	Volts	V_{SS}	—	0.8
TestMode	I_{IL}, Input Leakage	V_{IN} = 5.5V V_{IN} = 12.5V	uA uA	0 80	0.1 100	1.0 110
V_{PP}	I_{IL}, Input Leakage	V_{IN} = 5.5V 9<V_{IN}<5.5V V_{IN} = 12.5V	uA mA uA	0 0 80	0.1 8 100	1.0 10 110



Note: Programming should start with writing to address 0000.

Figure 21. EPROM Programming in Single Word Mode

DC CHARACTERISTICS (Continued)

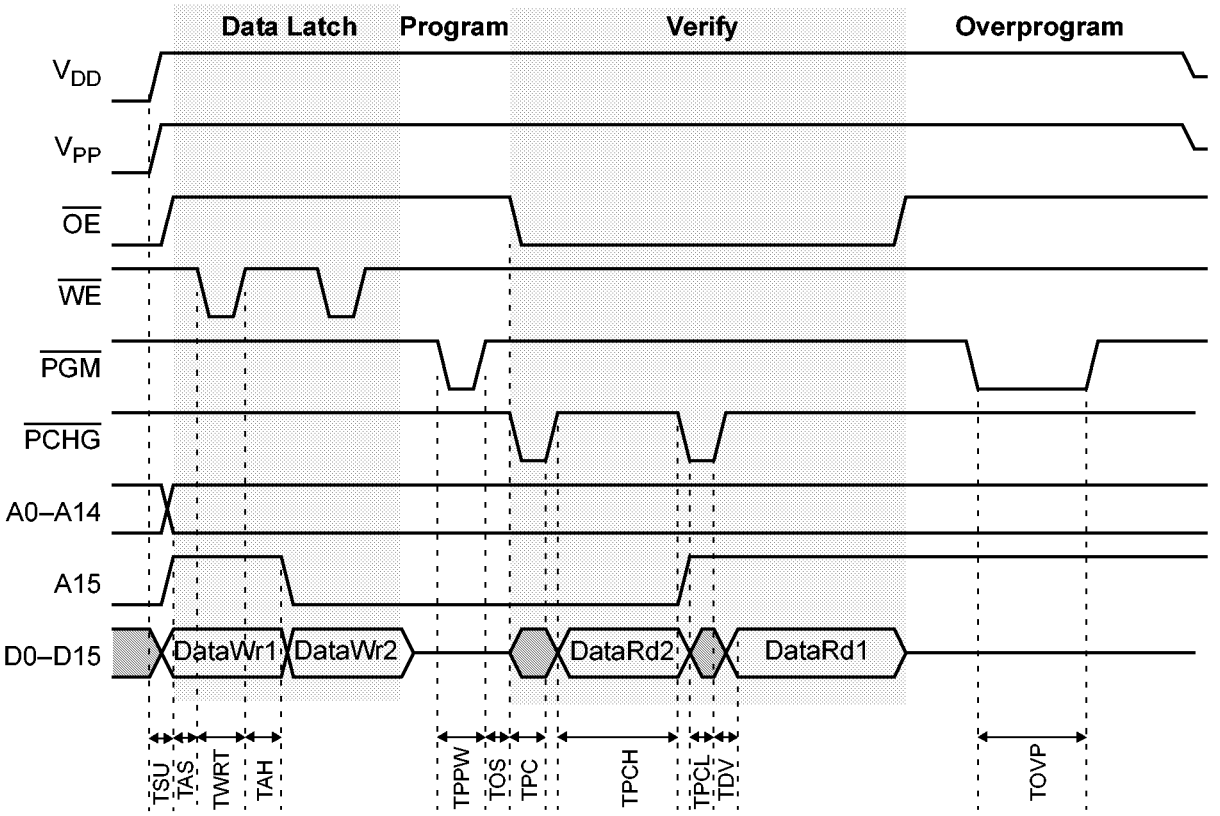
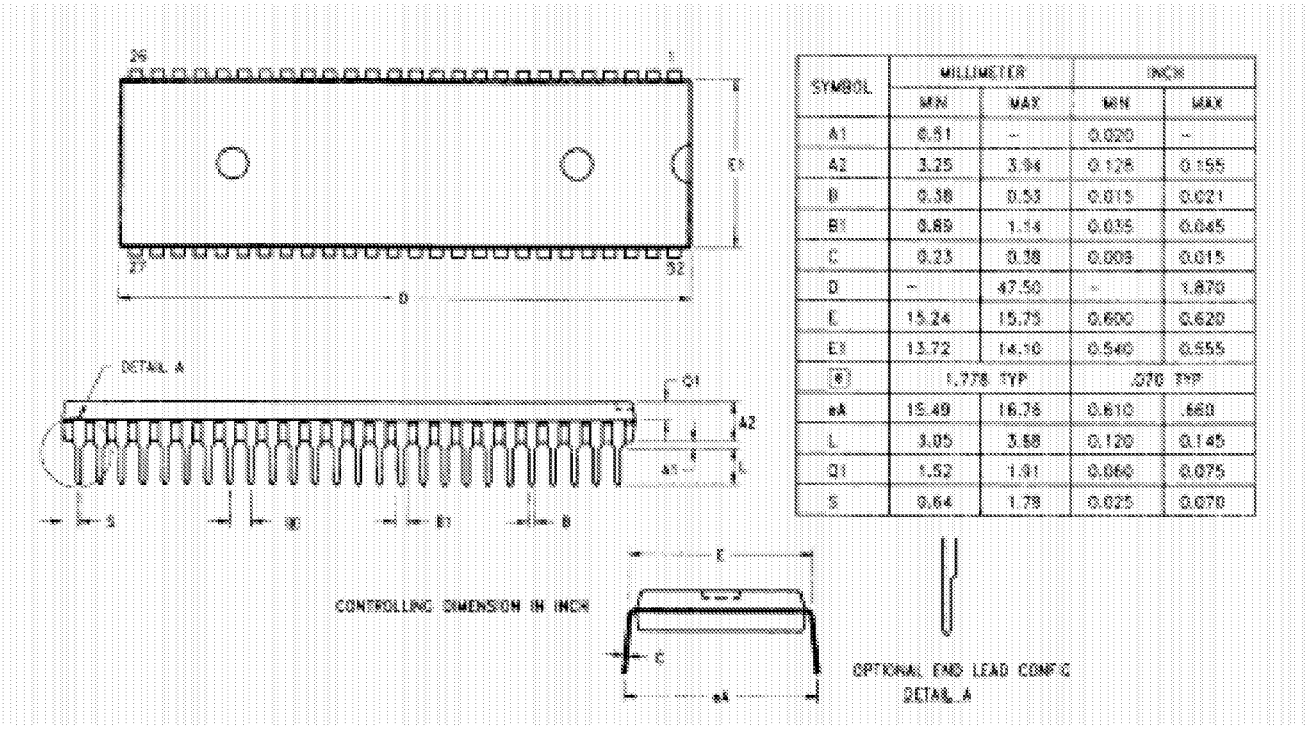


Figure 22. EPROM Programming In Double Word Mode

Table 58. Program/Verify Waveform Timing

Parameter	Description	Min	Typ	Max	Units
T_{SU}	V_{PP} CEB MODE TESTROM su	1	—	—	us
T_{AS}	Address set up	0.5	—	—	us
T_{DS}	Data set up	0.5	—	—	us
T_{WRT}	Write pulse width	300	—	—	ns
T_{AH}	Address 15 hold time after write	100	—	—	ns
T_{PPW}	Program pulse width	0.95	1.00	1.05	ms
T_{OVP}	Overprogram Pulse Width	2.85	3.00	3.15	ms
T_{OS}	$\overline{PGM}$ High to $\overline{OE}$ low	1	—	—	us
T_{PC}	$\overline{OE}$ to $\overline{PCHG}$	0	—	—	ns
T_{PCH}	$\overline{PCHG}$ High width	150	—	—	ns
T_{PCL}	$\overline{PCHG}$ Low width	300	—	—	ns
T_{DV}	$\overline{PCHG}$ High to data valid	150	—	—	ns

PACKAGE INFORMATION



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	–	0.020	–
A2	3.25	3.94	0.128	0.155
B	0.38	0.53	0.015	0.021
B1	0.89	1.14	0.035	0.045
C	0.23	0.38	0.009	0.015
D	–	47.50	–	1.870
E	15.24	15.75	0.600	0.620
E1	13.72	14.10	0.540	0.555
e	1.778 TYP		.070 TYP	
eA	15.49	16.76	0.610	.660
L	3.05	3.68	0.120	0.145
Q1	1.52	1.91	0.060	0.075
S	0.64	1.78	0.025	0.070

Figure 23. Z90371/6 52-Pin SDIP Package Dimensions

ORDERING INFORMATION

For fast results, contact your local ZiLOG sales office for assistance in ordering the part required.

Codes	
Package	P = Plastic DIP
Temperature	S = 0°C to +70°C
Speed	x = xx MHz
Environmental	C = Plastic Standard

Example:

Z 90376 12 P S C is a Z90376, 12 MHz, DIP, 0°C to 70°C, Plastic Standard Flow